

PCI-1002

Hardware User's Manual

Warranty

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1. Introduction

1.1 General Description

The PCI-1-1002L and PCI-1002H are high performance multifunction card, with A/D and digital I/O for PC and compatible computers in a 5V PCI slot. This family has the same features: one 12-bit 125K A/D converter, 16 channels D/I, 16 channels D/O, programmable interrupt source and support truly "Plug and Play". PCI-1002H/L provides 32 channels single-ended analog inputs or 16 channel differential analog inputs which are jumper selectable and the input channel number is also easily programmable by software. The PCI-1002L is the low-gain model which equipped a high speed PGA (programmable gain amp.) with programmable gain control 1,2,4,8 and PCI-1002H is the high-gain model which equipped a high-gain/high-resolution PGA with programmable gain control 1,10,100,1000. There are 16 channels of TTL compatible digital output port and 16 channel of TTL compatible digital input port. This series provide three programmable trigger methods : software trigger, pacer trigger and external trigger. The external trigger control can be programmable into one of the following trigger : post-trigger, pre-trigger, external pacer trigger. There are also several interrupt sources selectable: A/D conversion interrupt, pacer interrupt, external interrupt. This multifunction card also provides A/D buffer and high data transfer rate : 2.7M words per second in non-burst mode. This powerful A/D control mechanism offers the largest flexibility for various kinds of usage for users and the least I/O overhead for systems!! PCI-1002 series support fully "Plug and Play" under your system and can operating even on a full speed of PCI bus (66MHz), this important feature fits the latest version of computer I/O system and has the best performance. Besides, this series are low cost and are especially usefully for cost effect applications.

1.2 The Block Diagrams

The block diagram of PCI-1002 series is shown below :

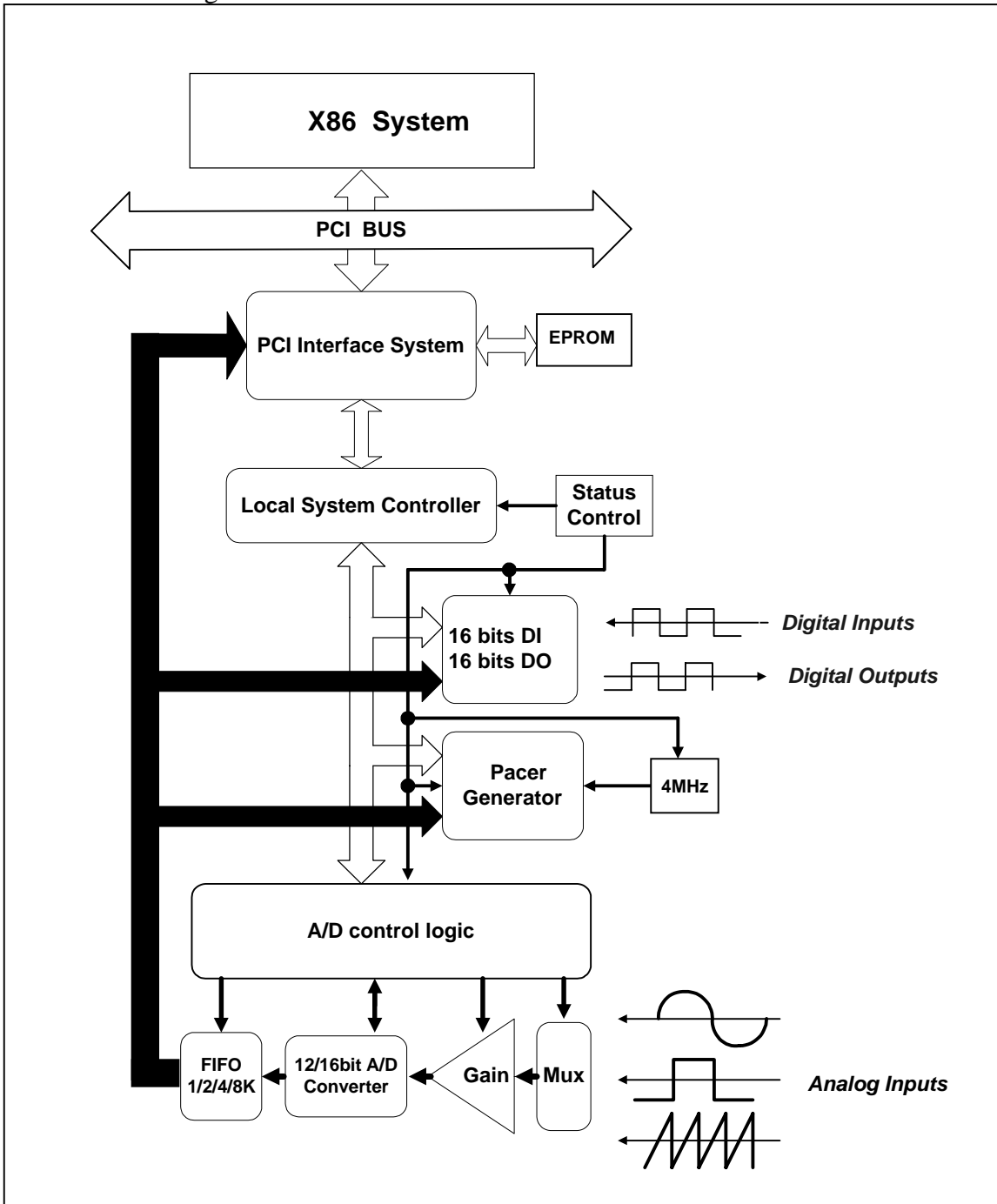


Figure 1-1. The PCI-1002 series block diagram.

1.3 Features

Following list the general feature of PCI1002 series, check section 1.4 for more details.

- Bus : 5V PCI (Peripherals Component Interface) bus.

- A/D :
 - 1 A/D converter with maximum 125Ksamples/second.
 - 32 single-ended / 16 differential programmable inputs for PCI-1002L/H.
 - Provides three different A/D trigger methods .
 - Provides three different external trigger methods.
 - Programmable gain control , programmable offset control.

- DIO :
 - 16 digital inputs and 16 digital outputs (TTL compatible) .
 - High speed data transfer rate : 2.7M word/sec (non-burst mode).

- Timer :
 - One 16-bit machine independent timer for software.
 - Two 16-bit pacer timer for A/D converter and interrupt.

1.4 Specifications

1.4.1 Power Consumption :

- +5V @960mA maximum, PCI-1002L/H
- Operating temperature : 0°C ~ +70°C

1.4.2 Analog Inputs

- Channels: (software programmable)
 - 32 single-ended inputs/16 differential inputs , jumper selectable.
- Gain control : (software programmable)
 - PCI-1002H: 1, 10, 100, 1000.
 - PIC-1002L: 1, 2, 4, 8.
- Input signal range :
 - PCI-1002L : Bipolar
Range: $\pm 10V, \pm 5V, \pm 2.5V, \pm 1.25V,$
 - PCI-1002H : Bipolar
Range: $\pm 10, \pm 1V, \pm 0.1V, \pm 0.01V$
- Input current: 250 nA max (125 nA typical) at 25 °C.
- Over voltage: continuous single channel to **70Vp-p**
- Input impedance:
PCI-1002H/L: $10^{10}\Omega // 6pF$

1.4.3 D/I and D/O

- Channels : 16 channels DI, 16 channels DO.
- DO : Digital output port
 - Output level : TTL compatible
 - Output current : $I_{oh} = 0.5mA$, $I_{ol} = 8mA$
- DI : Digital input port
 - Input level : TTL compatible
 - Input current : $50 \cdot A$ (max).

1.4.4 A/D Trigger Methods

- Trigger-methods :
 - Software trigger.
 - Pacer trigger : 16-bit programmable timer/counter.
 - External trigger : pre-trigger, post-trigger, external pacer trigger.

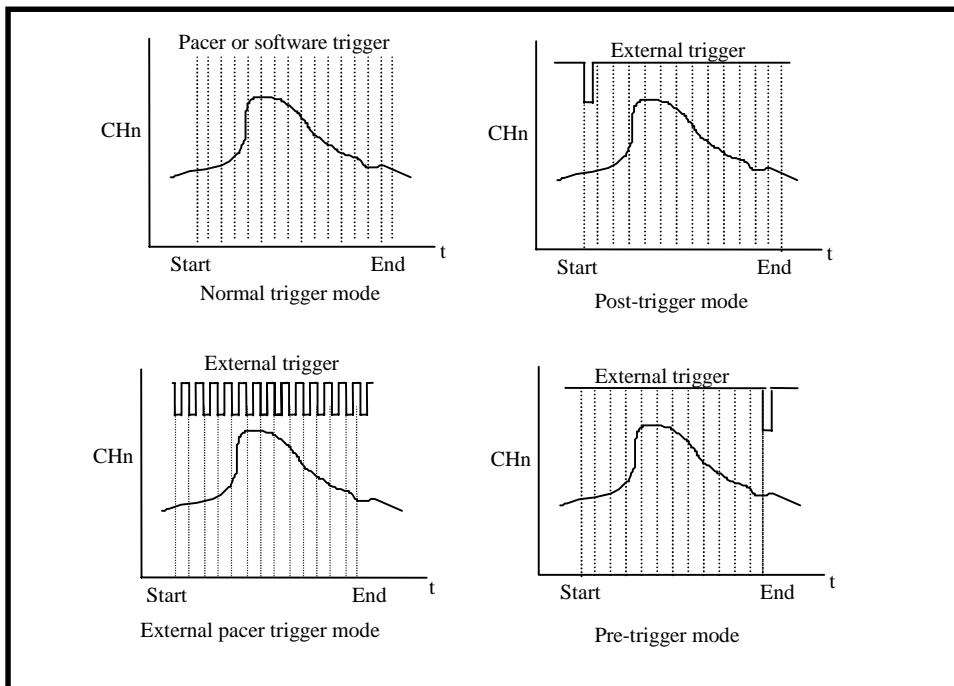


Figure 1-2. Trigger methods of PCI-1002.

1.4.5 Interrupt Channel

- Interrupt : INTA (Automatically assigned by PCI-initiator).
- Enable/Disable : Via PCI control register and add-on control register.
- Interrupt source : (Selected by on-board control register)
 1. A/D conversion interrupt.
 2. Pacer 0 interrupt.
 3. Pacer 1 interrupt.
 4. External interrupt.

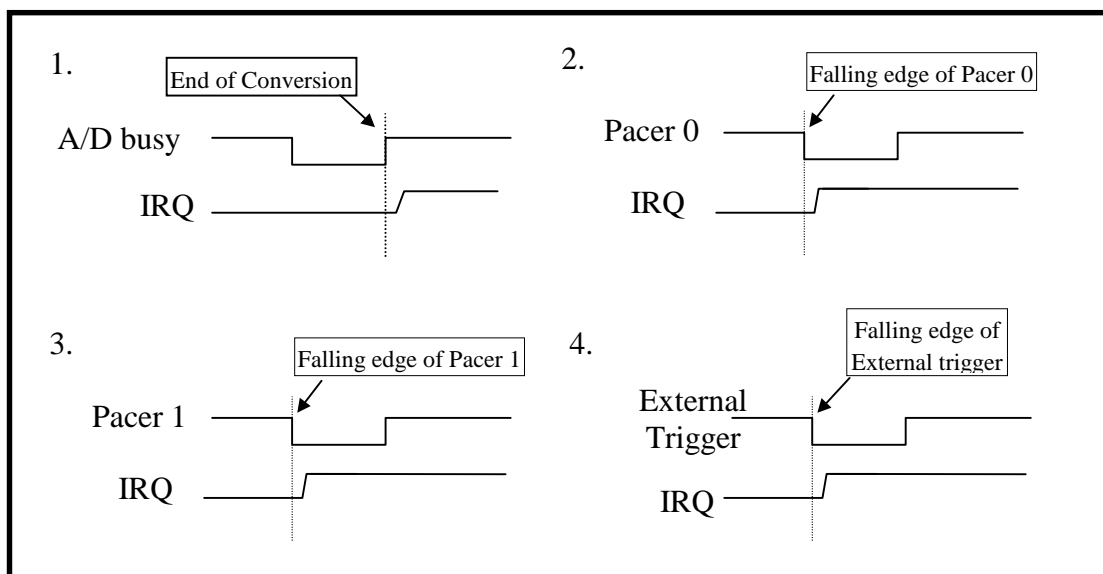


Figure 1-3. Programmable interrupt source.

1.4.6 Programmable Timer/Counter

- Type : 82C54 -8 programmable timer/counter
- Timers : Timer 1 for Pacer trigger and interrupt,
Timer 2 for External trigger and interrupt,
Timer 3 for software machine independent timer.
- Input Clock: 4 M Hz.

1.5 Applications

- Signal analysis.
- FFT & frequency analysis.
- Transient analysis.
- Speech analysis.
- Temperature monitor.
- Vibration analysis.
- Energy management.
- Other industrial and laboratory measurement and control.

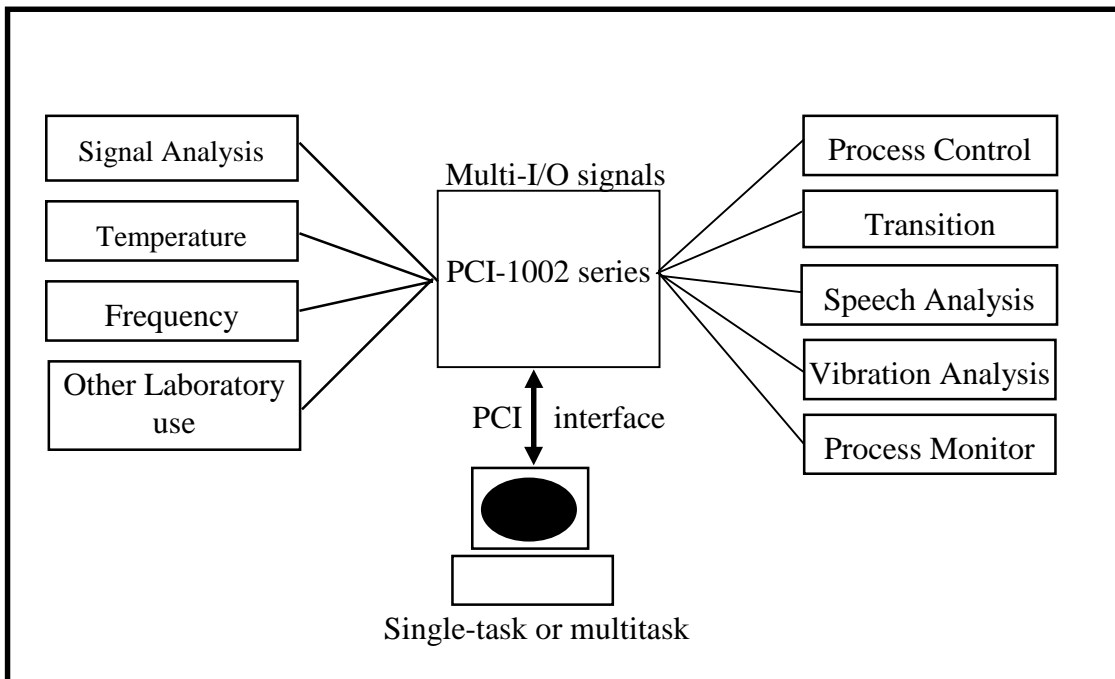


Figure 1-4. PCI-1002 series multifunction cards.

1.6 Product Check List

In addition to this manual, the package includes the following items:

- PCI-1002L/1002H multifunction card.
- One utility/library diskette.
- Software menu.

Attention !

If any of these items is missing or damaged, please contact your local field agent. Save the shipping materials and carton in case you want to ship or store the product in the future.

2. Hardware Configuration

2.1 Board Layout

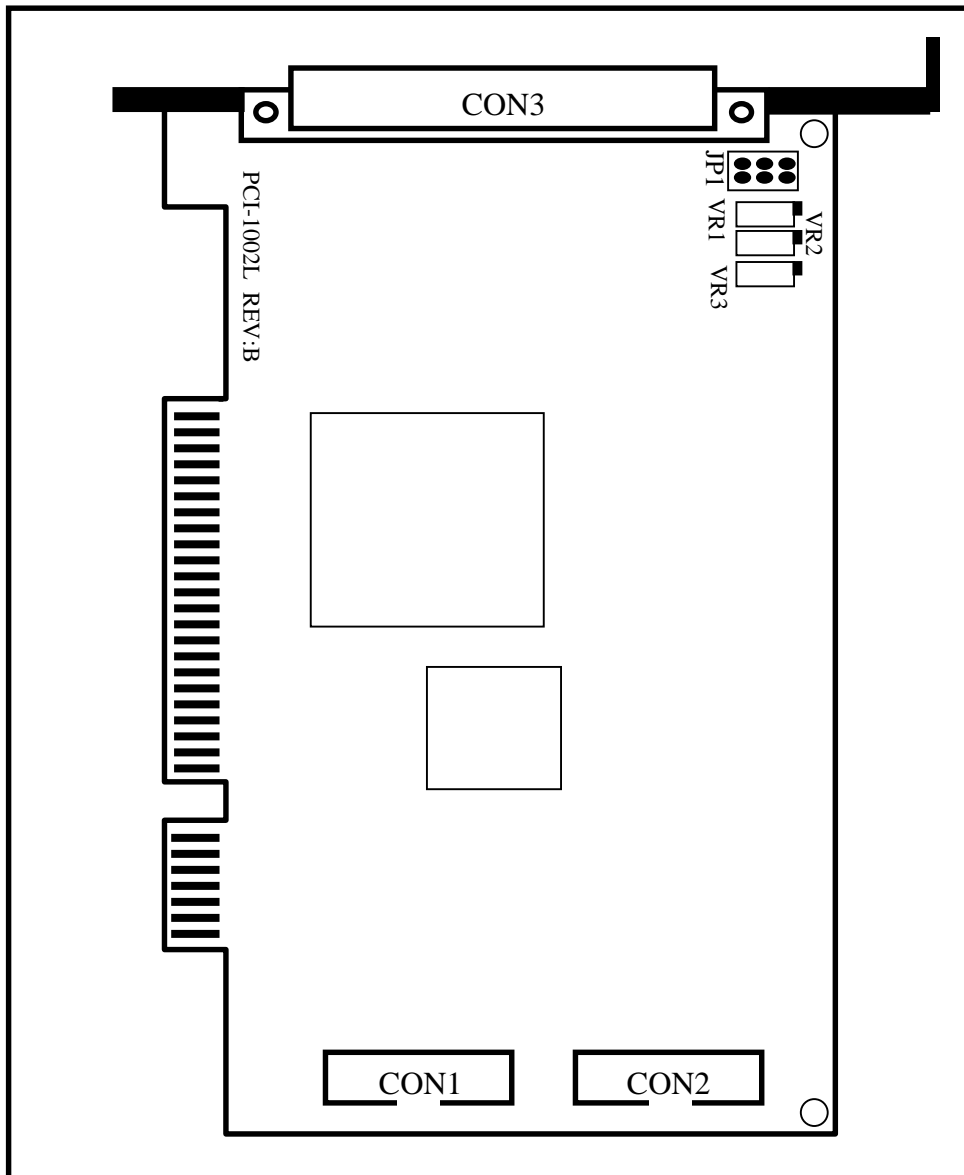


Figure 2-1. PCI-1002 board layout.

2.2 System Block

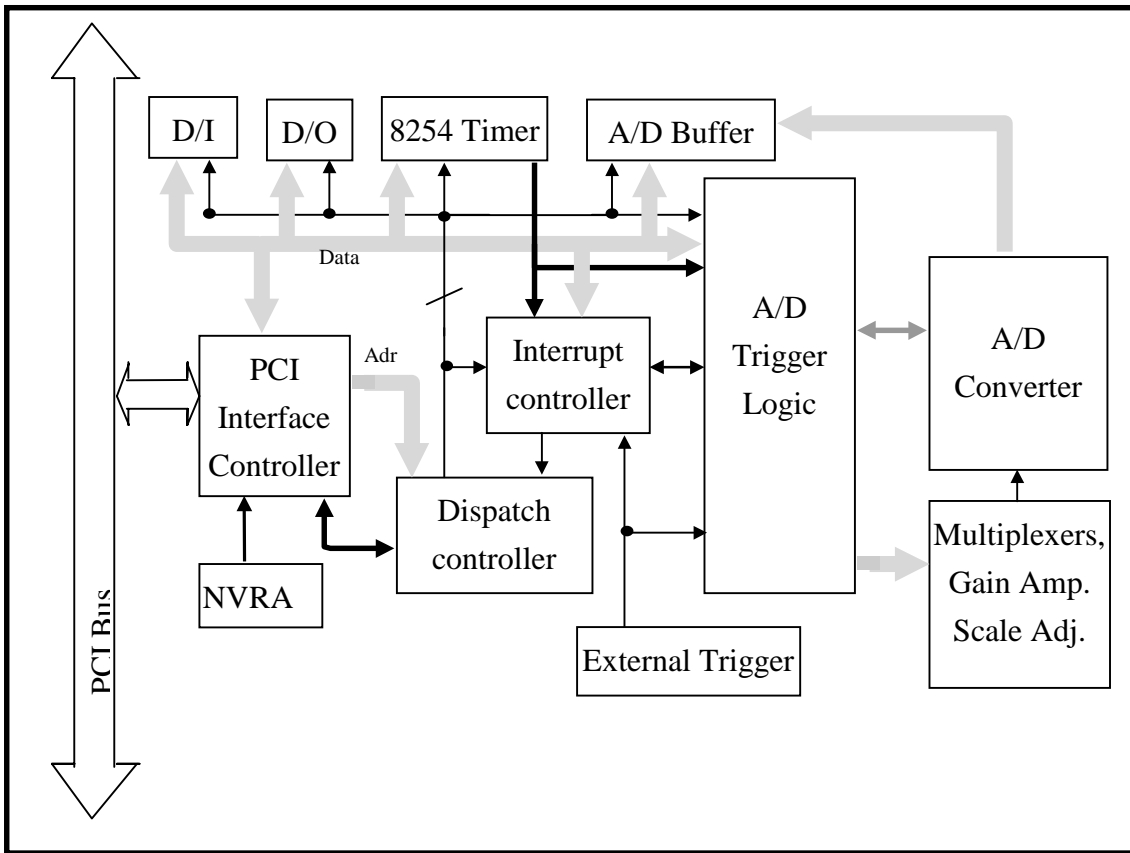


Figure 2-2. PCI-1002 System Function Block.

2.3 Base Address

The base address of PCI-1002 is automatically assigned by the system after power on or after hardware reset signal. There are three address spaces used by PCI-1002, one memory space and two I/O space. **User should not use the control registers that mapped in the memory space!!** Following is the abbreviate list of the registers :

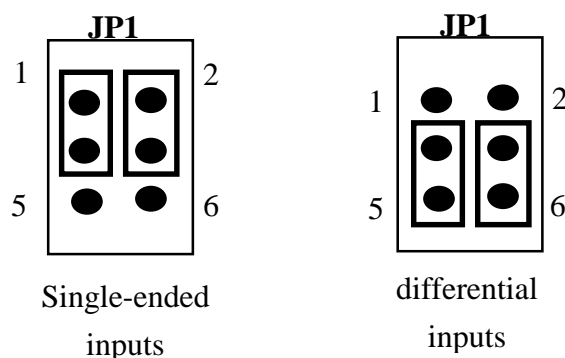
Section	Name	Type	Length	Descriptions
[*] 0	PCI controller	Memory	128 Bytes	The PCI interface controller registers.
1	PCI controller	I/O	128 Bytes	The PCI interface controller registers.
2	Add-on registers	I/O	64 Bytes	Add-on circuit control registers.

[*] : The section should not be used in the normal operation.

Note : Although the I/O address and memory address of PCI-1002 can be re-assigned by PCI mechanism #2, users are not encourage to change the I/O address!

2.4 Jumper Setting

There is only one jumper in PCI-1002. JP1 is used to select the analog input type. For single-ended inputs, users should connected pin1,3 and pin2,4. For differential inputs, pin3,5 and pin4,6 should be connected.



2.5 The Connectors

CN1 : Digital output connector pin assignment .

Pin	Name	Pin	Name
1	Digital output 0	2	Digital output 1
3	Digital output 2	4	Digital output 3
5	Digital output 4	6	Digital output 5
17	Digital output 6	8	Digital output 7
9	Digital output 8	10	Digital output 9
11	Digital output 10	12	Digital output 11
13	Digital output 12	14	Digital output 13
15	Digital output 14	16	Digital output 15
17	PCB ground	18	PCB ground
19	PCB +5V	20	PCB +12V

1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20

CN2 : Digital input connector pin assignment.

Pin	Name	Pin	Name
1	Digital input 0	2	Digital input 1
3	Digital input 2	4	Digital input 3
5	Digital input 4	6	Digital input 5
17	Digital input 6	8	Digital input 7
9	Digital input 8	10	Digital input 9
11	Digital input 10	12	Digital input 11
13	Digital input 12	14	Digital input 13
15	Digital input 14	16	Digital input 15
17	PCB ground	18	PCB ground
19	PCB +5V	20	PCB +12V

CN3 : Analog input/output connector pin assignment. (for PCI-1002H/L)

Pin	Name	Pin	Name
1	Analog input 0/0+	20	Analog input 16/0-
2	Analog input 1/1+	21	Analog input 17/1-
3	Analog input 2/2+	22	Analog input 18/2-
4	Analog input 3/3+	23	Analog input 19/3-
5	Analog input 4/4+	24	Analog input 20/4-
6	Analog input 5/5+	25	Analog input 21/5-
7	Analog input 6/6+	26	Analog input 22/6-
8	Analog input 7/7+	27	Analog input 23/7-
9	Analog input 8/8+	28	Analog input 24/8-
10	Analog input 9/9+	29	Analog input 25/9-
11	Analog input 10/10+	30	Analog input 26/10-
12	Analog input 11/11+	31	Analog input 27/11-
13	Analog input 12/12+	32	Analog input 28/12-
14	Analog input 13/13+	33	Analog input 29/13-
15	Analog input 14/14+	34	Analog input 30/14-
16	Analog input 15/15+	35	Analog input 31/15-
17	Analog ground	36	N.C.
18	N.C.	37	Digital ground
19	External trigger		

Note :

1. Once differential analog input is selected (JP1 3-5, 4-6), Pin 1-16 will be taken as the positive inputs and Pin 20-35 are taken as the negative inputs of the channel.
2. ' N.C. ' is the abbreviation of "Not Connected".

2.6 I/O Register Address

The list of PCI-1002 registers is given below, the address of each register is simply got from adding the offset to the base address of the corresponding section. More detail descriptions of the registers will be shown in the following

text and the software manual.

Section	offset	Name	Access	Length
1	4ch	PCI interrupt control register	R/W	8/16/32 bits
2	00h	8254 timer1	R/W	8/16/32 bits
	04h	8254 timer2	R/W	8/16/32 bits
	08h	8254 timer3	R/W	8/16/32 bits
	0Ch	8254 control register	W	8/16/32 bits
	10h	Analog input channel control register	W	8/16/32 bits
	10h	Status register	R	8/16/32 bits
	14h	Analog input gain control register	W	8/16/32 bits
	18h	General control register	W	8/16/32 bits
	1Ch	A/D software trigger	W	8/16/32 bits
	1Ch	Clear Interrupt	R	8/16/32 bits
	20h	Digital output register	W	16/32 bits
	20h	Digital input register	R	16/32 bits
	30h	A/D data register	R	16/32 bits

2.6.1 Section 1

Although there are 128 I/O ports used by the on-board PCI interface controller, only one register is used in the real applications!! Users should keep the other registers from being modified! The PCI interrupt control register (4Ch) control the interrupt generated to your system. The register is set to “disable interrupt” after power-on or hardware reset signal, thus no interrupt will be generated before this register is activated even if user enable the add-on interrupt! In order to enable the PCI-interrupt, always write 0x43 to this register. Write 0x03 to this register if you want to disable the PCI interrupt !!.

Following is the format of the PCI interrupt control register :

Bit 31-Bit 7	Bit6	Bit5-Bit3	Bit2	Bit1-Bit0
Not used	Interrupt Enable	Not used	Interrupt Flag	Interrupt Select

Bit 6 : Write an ‘1’ to enable the PCI-interrupt and a ‘0’ to disable PCI interrupt.

Bit 2 : This bit is readable but can not be written. A ‘1’ indicates that Add-on has generate interrupt, ‘0’ means that add-on doesn’t generate interrupt.

Bit1-0 : Always write 1 to these two bits.

Note :

1. Because PCI-1002 supports “Plug and Play”, the interrupt number will be automatically assigned by your system. User should use the standard PCI mechanism or use the software in our library to find out the interrupt number.
2. If your system supports “Shared IRQ”, thus several peripherals will share the same IRQ in the same time. You must use Bit-2 to find out if this IRQ was generated from your PCI-1002 !!!
3. For more information about the PCI interrupt control, please refers to the user reference manual of PLX-9050.

2.6.2 Section 2

This section is used by the add-on control logic. 64 bytes of I/O locations are used. Their detail descriptions are shown below

2.6.2.1 The 8254 registers

8254, programmable timer/counter, is used to generate periodic A/D trigger signal, periodic interrupt signal and the machine independent timer for PCI-1002. Address 00h, 04h, 08h and 0Ch are used to control the 8254. For more details about the programming information please refer to Intel's "Microsystem Components Handbook". For more information about the control mechanism of PCI-1002 please refers to chapter 3.

2.6.2.2 The DI / DO register

Address 20h is used for DI / DO ports. Write to this port will write data to DO register. Read from this port will read the data from DI.

2.6.2.3 The A/D buffer

Address 30h is used for A/D buffer. Only read operation is available in this address. Read from this port will read the data from A/D buffer. The format of A/D buffer is :

Bit15-12	Bit11-0
Analog input channel	A/D data

Bit15-12 : The channel number of analog input. Only lower 4 bits of channel number are shown in this register.

Bit11-0 : The A/D data.

2.6.2.4 The status register

Address 20h is used by the status register. A read from this address will get the data from the status register. The format of status register is :

Bit7-6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Gain control	8245 Timer 2	8245 Timer 1	8245 Timer 3	Reserved	Analog input type	A/D busy

- Bit 7-6 : Current A/D gain control.
- Bit 5 : Output of 8254 timer 2.
- Bit 4 : Output of 8254 timer 1.
- Bit 3 : Output of 8254 timer 3.
- Bit 2 : Reserved. Used for hardware testing.
- Bit 1 : Analog input type, '1' indicated that analog input type is single-ended and '0' indicated analog input is differential.
- Bit 0 : A/D busy signal. '0' indicates busy, A/D is under conversion. '1' indicates not busy, A/D is complete conversion and is idle now.

2.6.2.5 The A/D software trigger register

Write to this port (1Ch) will generate an A/D trigger pulse signal .

Note : Although user can performs a very fast trigger (more than the speed of A/D controller, 125K) by this method, a reasonable delay time should be add between two triggers.

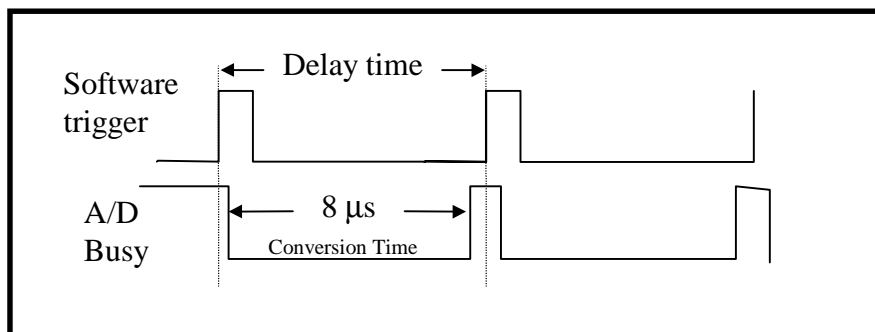


Figure 2-3. Software trigger delay time.

2.6.2.6 Clear interrupt

A read from 1Ch will clear the add-on interrupt.

2.6.2.7 The analog input selection register

Address 20h is used by the analog input channel selection register and address 24h is used by the analog gain control selection register. Write 0-31 to port 20h to select the channel number (for differential input, write 0-15). Write 0-3 to port 24h to select the gain control.

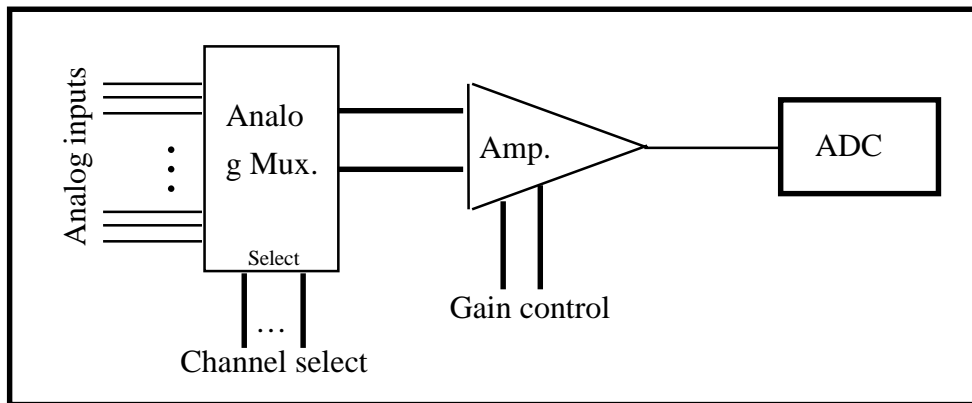


Figure 2-4. Analog input control.

Note :

1. For single ended inputs, channel 0-31 are available. For differential inputs, channel 0-15 are available. The input numbers which are more than the available channel will be discard. Thus, for single-ended inputs, only the last 5 bits are taken as the channel number. And for differential inputs, only the last 4 bits are taken as the channel number.
2. Only the last two digit are taken as the gain control code. The gain control code and the corresponding gain is :

For PCI-1002L :

Gain code	[0 0]	[0 1]	[1 0]	[1 1]
Gain	1	2	4	8

For PCI-1002H :

[Bit1,Bit0]	[0 0]	[0 1]	[1 0]	[1 1]
Gain	1	10	100	1000

3. These registers are set to 0 after power-on or hardware reset signal.

2.6.2.8 The general control register

General control register (18h) is used to control the add-on interrupt signal source and the A/D trigger method. The format of this register is :

Bit4-2	Bit 1-0
Interrupt source selection register	A/D trigger method selection register

2.6.2.8.1 Interrupt source selection

There are four interrupt selectable for PCI-1002 (see section 1.4.4).

[Bit4,Bit3,Bit2]	Descriptions
[0, 0, 0]	No interrupt source, disable all interrupts.
[0, 0, 1]	Interrupt after A/D complete conversion.
[0, 1, 0]	Interrupt after 8254 timer 0 falling.
[0, 1, 1]	Interrupt after external trigger falling.
[1, 0, 0]	Interrupt after 8254 timer 1 falling .
Others	No interrupt source, disable all interrupts.

Note: Bit 4-2 of general control register is set to 0 after hardware reset.

2.6.2.8.2 Trigger method selection

There are several trigger methods can be selected by users (see section 1.4.5):

[Bit1,Bit0]	Descriptions
[0, 0]	General trigger mode. 8254 timer 0 trigger (internal pacer trigger) or software trigger.
[0, 1]	External clock trigger mode.
[1, 0]	Pre-trigger mode.
[1, 1]	Post-trigger mode.

Note :

1. In general trigger mode, both 8254 timer 0 and software trigger are take as the A/D trigger signals. Under this mode, 8254 timer 0 and software trigger should not working in the same time!! This means **users should not generate software trigger while 8254 timer 0 is activated !!**
2. In external clock trigger mode, external trigger input is taken as the A/D trigger signal. One falling edge of the external trigger input will generate one A/D trigger.
3. Pre-trigger mode is used for pre-trigger method, it is working incorporated with the 8254 timer 1. User should first setup 8254 timer 1 properly then set the trigger mode to pre-trigger. Once pre-trigger mode has been activated, it will automatically turn on 8254 timer 1 and start to performs A/D triggers. It will be continued until the A/D trigger logic receives a falling of external trigger signal. Any change to the trigger mode selection will turn off pre-trigger mode.
4. Post-trigger mode is used for post-trigger method, it is working incorporated with the 8254 timer 1. User should first setup 8254 timer 1 properly then set the trigger mode to post-trigger. Once post-trigger mode has been activated, it will automatically turn off 8254 timer 1 until it receives a falling of external trigger signal. Any change to the trigger mode selection will turn off post-trigger mode.
5. The A/D trigger selection are set to 0 after power-on or hardware reset.

3. Function Operation

3.1 Digital I/O

The PCI-1002 series provide 16 digital input channels and 16 digital output channels. All levels are TTL compatible. The connections diagram and block diagram are given below :

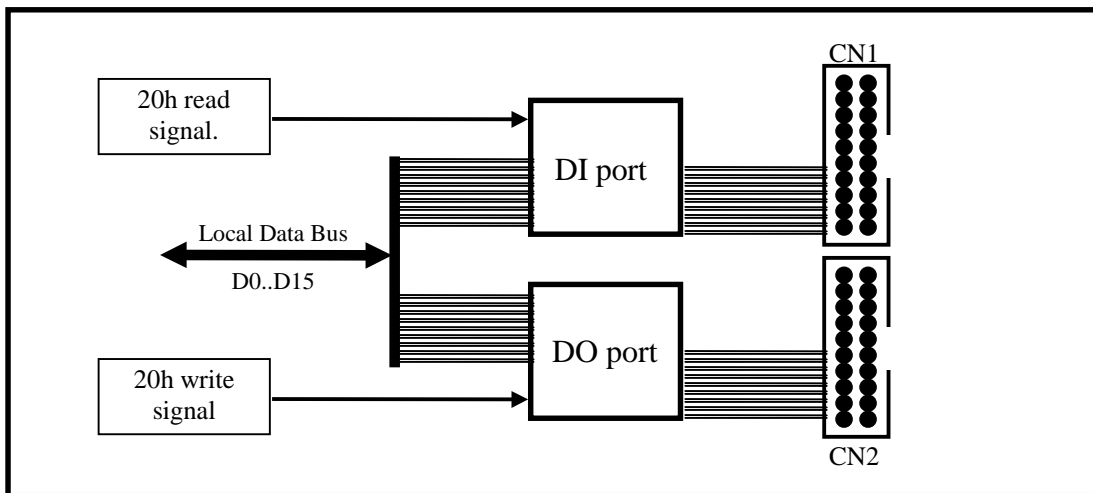


Figure 3.1. DIO function diagram.

3.2 The 8254 Timer

The PCI-1002 series provide 3 independent 16-bit timer/counter, each timer has different functions. The block diagram is given as below:

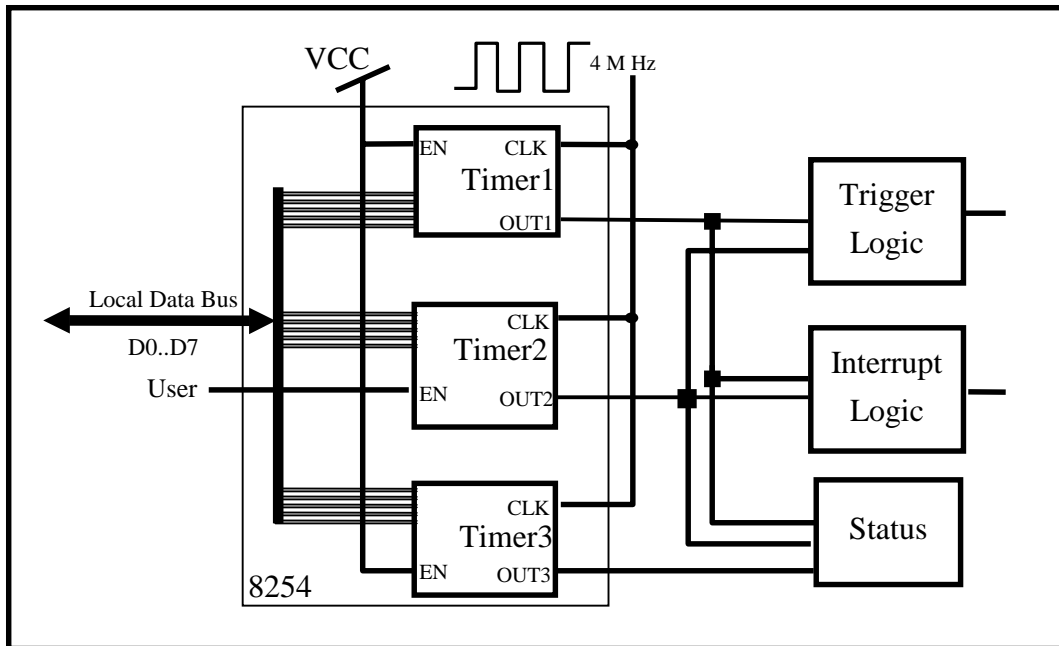


Figure 3-2. 8254 control diagram.

3.3 The A/D trigger

The A/D trigger is controlled by on-board A/D trigger controller. The function diagram of A/D trigger is shown below :

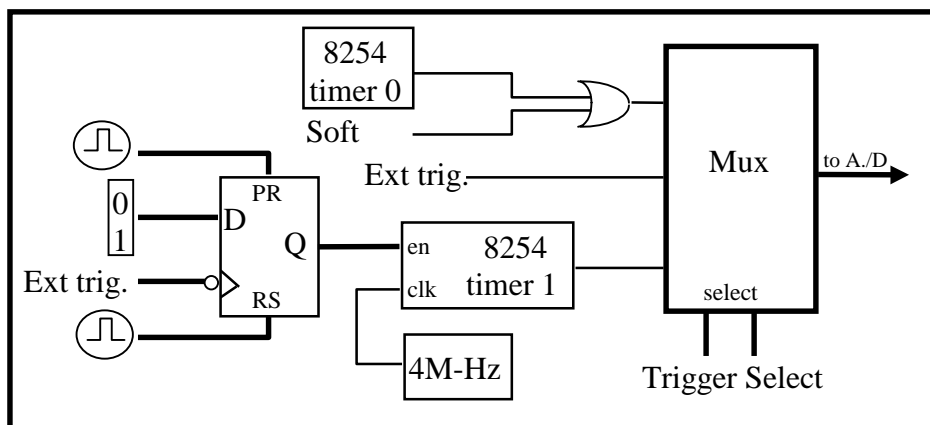
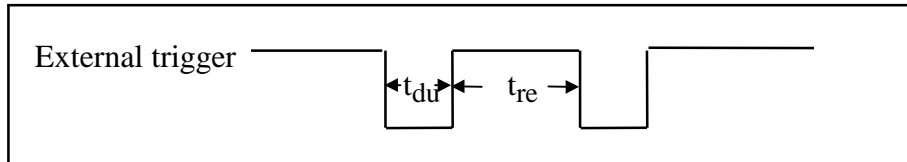


Figure 3-3. A/D trigger controller.

A/D trigger logic receives the external trigger and performs the correct A/D trigger function. In order to be recognized by the A/D trigger controller, the external trigger signals must be a TTL compatible signal and must have the minimum duration of pulse width to avoid noise. This signal must satisfy the following specifications :



Symbol	Name	Minimum	Maximum
t_{du}	Duration time	40ns	•
t_{re}	Recover time	100ns	•

Note: The PCI-1002 is designed only for the time sensitive trigger (trigger is dependent only on the time of the falling edge of external trigger signal). For a level sensitive external trigger (trigger is dependent only on the level of the input signals), users can make the following circuit outside the PCI-1002 :

