

**TECHNICAL USER'S MANUAL FOR:**

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# MICROSPACE<sup>®</sup>

PERIPHERAL BOARD

## MSMS104+ AD7880 SCSI card

## MSME104+ 82C559 LAN100 card



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		V0.2	09.99 JM	Designs added
	V1.3	V0.3	05.2000 STP	Minor corrections
	V1.4	V0.4	03.2001 BEL/STP	LAN Boot feature added, new Logo and address added, etc
				...

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# 1      **PREFACE**

This manual is for integrators and programmers of systems based on the MicroSpace card family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime. If errors are found, please notify DIGITAL-LOGIC AG at the address shown on the title page of this document, and we will correct them as soon as possible.

## 1.1    ***How to use this manual***

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MicroSpace-PC. It provides instructions for installing and con-figuring the MSMS/E104 board, and describes the system and setup requirements.

## 1.2    ***Trademarks***

Chips & Technologies	SuperState R
MicroSpace, MicroModule	DIGITAL-LOGIC AG
DOS Vx.y, Windows	Microsoft Inc.
PC-AT, PC-XT	IBM
NetWare	Novell Corporation
Ethernet	Xerox Corporation
DR-DOS, PALMDOS	Digital Research Inc. / Novell Inc.
ROM-DOS	Datalight Inc.

## 1.3    ***Disclaimer***

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## 1.4    ***Who should use this product***

- Electronic engineers with know-how in PC-technology.
- Without electronic know-how we expect you to have questions. This manual assumes, that you have a general knowledge of PC-electronics.
- Because of the complexity and the variability of PC-technology, we can't give any warranty that the product will work in any particular situation or combination. Our technical support will help you to may get a solution.
- Pay attention to the electrostatic discharges. Use a CMOS protected workplace.
- Power supply OFF when you are working on the board or connecting any cables or devices.

<p style="text-align: center;"><b>This is a high technology product. You need know-how in electronics and PC-technology to install the system !</b></p>
---

## **1.5 Recycling Information**

### **Hardware:**

- **Print:** epoxy with glass fiber  
wires are of tin-plated copper
- **Components:** ceramics and alloys of gold, silver  
check your local electronic recycling

### **Software:**

- **no problems:** re-use the diskette after formatting

## **1.6 Technical Support**

1. Contact your local Digital-Logic Technical Support in your country.
2. Use Internet Support Request form on <http://www.digitallogic.com> -> support -> support request form
3. Send a FAX or an E-mail to DIGITAL-LOGIC AG with a description of your problem.

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smartModule DesignIn Center  
Nordstr. 11/F  
CH-4542 Luterbach (SWITZERLAND)  
Fax: ++41 32 681 58 01  
E-Mail: [support@digitallogic.com](mailto:support@digitallogic.com)  
Internet: [www.digitallogic.com](http://www.digitallogic.com)

- ➔ Support requests will only be accepted with detailed informations about the product (BIOS-, Board-version) !

## **1.7 Limited Warranty**

DIGITAL-LOGIC AG warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original product purchaser and is not transferable.

During the one year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

**Before returning any product for repair, customers are required to contact the company.**

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Neither, if the user has not enough knowledge of these technologies or has not consulted the product manual or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

Except, as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

## 2 OVERVIEW

### 2.1 Ordering information

MSMS104+	SCSI option
MSME104+	LAN100 option
Option	PC104 connector assembled

### 2.2 General information

#### **BUS:**

Standard:	PC/104+
Size:	32Bit PCI

#### **Power Supply:**

Power:	Working: 5volt / 1W
--------	---------------------

#### **Physical Characteristics:**

Dimensions:	Length: 90mm
	Width: 96mm
	Height: 15mm

#### **Operating Environment:**

Relative humidity:	5 - 90% non condensing		
Vibration:	5 to 2000 Hz		
Shock:	10g		
Temperature:	Operating:	Standard version:	-25°C to +70 °C
		Industry version:	-25°C to +85°C (ask DIGITAL-LOGIC AG)
	Storage:		-55°C to 85°C

## **2.3    SCSI**

**SCSI Interface:**

Controller:	AIC7880	From ADAPTEC
Enhanced BIOS:	yes 3.1	
Memory:	none	
Interface:	50pin SCSI connector	
Driver:	From ADAPTEC or OS software	

## **2.4    LAN100BASE-T**

**LAN100  
Interface:**

Controller:	82C559	From INTEL
Enhanced BIOS:	yes	
Memory:	512kB	
Interface:	RJ45 LAN	
Driver:	From ADAPTEC or OS software	

**Any information is subject to change without notice.**

## 3 PC/104 BUS SIGNALS

### AEN, output

Address Enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle , high = DMA Cycle**

### BALE, output

Address Latch Enable is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17..23. The SA0..19 address lines latched internally according to this signal. BALE is forced high during DMA cycles.

### /DACK[0..3, 5..7], output

DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are **active low**. This signal indicates that the DMA operation can begin.

### DRQ[0..3, 5..7], input

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQ0 through DRQ3 will perform 8-Bit DMA transfers; DRQ5-7 are used for 16 accesses.

### /IOCHCK, input

IOCHCK/ provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error, high = normal operation**

### IOCHRDY, input

I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held low for no more than 2.5 microseconds. **low = wait, high = normal operation**

### /IOCS16, input

I/O 16 Bit Chip Select signals the system board that the present data transfer is a 16-Bit, 1 wait-state, I/O cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA15-SAO (not /IOR or /IOW) when AEN is not asserted. In the 8 Bit I/O transfer, the default transfers a 4 wait-state cycle.

### /IOR, input/output

I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is **active low**.

### /IOW, input/output

I/O Write instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

**IRQ[ 3 - 7, 9 - 12, 14, 15], input**

These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request.

**/Master, input**

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a /DACK.

**/MEMCS16, input**

MEMCS16 Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-Bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA.

**/MEMR input/output**

These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

**/MEMW, input/output**

These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low**.

**OSC, output**

Oscillator (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100µs after reset is inactive.

**RESETDRV, output**

Reset Drive is used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is active high. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

**/REFRESH, input/output**

These signals are used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel. These signals are **active low**.

**SAO-SA19, LA17 - LA23 input/output**

Address bits 0 through 19 are used to address memory and I/O devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SA0 through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16 MBytes range. These signals are generated by the microprocessors or DMA controllers. They may also be driven by other microprocessor or DMA controllers that reside on the I/O channel. The SA17-SA23 are always LA17-LA23 address timings for use with the MSCS16 signal. This is advanced AT96 design. The timing is selectable with jumpers LAXx or Saxe.

**/SBHE, input/output**

Bus High Enable (system) indicates a transfer of data on the upper byte of the data bus, XD8 through XD15. Sixteen-Bit devices use /SBHE to condition data-bus buffers tied to XD8 through XD15.

**SD[O..15], input/output**

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. DO is the least-significant Bit and D15 is the most significant Bit. All 8-Bit devices on the I/O channel should use DO through D7 for communications to the microprocessor. The 16-Bit devices will use DO through D15. To support 8-Bit device, the data on D8 through D15 will be gated to DO through D7 during 8-Bit transfers to these devices; 16-Bit microprocessor transfers to 8-Bit devices will be converted to two 8-Bit transfers.

**/SMEMR input/output**

These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

**/SMEMW, input/output**

These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low**.

**SYSCLK, output**

This is a 8 MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 66% duty cycle. This signal should only be used for synchronization.

**TC output**

Terminal Count provides a pulse when the terminal count for any DMA channel is reached. The TC completes a DMA-Transfer. This signal is expected by the onboard floppy disk controller. Do not use this signal, because it is internally connected to the floppy controller.

**/OWS, input**

The Zero Wait State (/OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-Bit device without wait cycles, /OWS is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-Bit device with a minimum of one-wait states, /OWS should be driven active one system clock after the Read or Write command is active, gated with the address decode for the device. Memory Read and Write commands to an 8-Bit device are active on the falling edge of the system clock. /OWS is **active low** and should be driven with an open collector or tri-state driver capable of sinking 20mA.

**12V +/- 5%**

used only for the flatpanel supply and BIAS generation.

**GROUND = 0V**

used for the entire system.

**VCC, +5V +/- 0.25V**

separate for logic and harddisk/floppy supply.

**3.1 Expansion Bus**

The bus is the standard PCI bus.

## **4 100/10 ETHERNET LAN**

Required programs and drivers are located on our CD in the directory `x:\DRIVERS\NETWORK\INTEL\`

### **4.1 Intel 82559 Ethernet chip**

- Create a directory `C:\LAN100` on your harddisk.
- Copy the programs and drivers of `x:\DRIVERS\NETWORK\INTEL\82559\` onto your HD.

#### **4.1.1 Installation example for MSDOS Novell 4.11**

- run "setup.exe" in the directory `c:\lan100\...`
- choose "install network drivers"
- choose "Novell"
- choose "DOS odi client"
- choose "continue installation"
- the settings in this menu are optional (preferred server (optional); frame type = 802.2)
- press F10
- select a name for the directory of your choice, for example: "`c:\network`"
- press enter
- choose "modify autoexec.bat"
- exit setup

Change the file "startpro.bat" of `c:\network` in:

```
c:
cd \network
ls
e100bodi
ipx.odi
cd dos
vlm
cd \
```

Copy the directory `x:\drivers\network\intel\client\dos` from our product CD into the directory `c:\network\`

#### **4.1.2 Driver installation WINDOWS 95**

- Copy Intel Pro100+ drivers on HDD (`x:\drivers\network\intel\82559`).
- De-install all network drivers under Windows95 in system and software folders and restart Windows. Networkcard Pro10 PCI will be auto-detected and all drivers can be installed (of the copied directory).
- Restart Windows and there is a failure message.
- Call up the networkcard-preferences in the devicemanager and update the drivers.
- Choose the Intel 8255x-based PCI Ethernet Adapter (10/100) out of the list.
- Shut down Windows and switch off the power supply unit.
- Boot up again and the network is installed.

### **4.1.3 Driver installation WINDOWS 98SE**

- Update the driver from the Intel® PRO/10+PCI device in the device manager.
- Choose the option "select list with drivers".
- Choose the "Intel 8255xx based Ethernet PCI Adapter(10/100)".
- Go on. If you get a failure report, press ok.
- If the PC hangs, switch off/on the power.
- After reboot, you must activate the Intel 8255xx driver in the device manager.

### **4.1.4 Driver installation WINDOWS NT**

Please note, that one has to write the whole directory path, when NT asks for the new driver installation. Windows NT does not search automatically for a new directory.

Installing another driver:

Select the path, where the driver is located, especially where the OEM- inf file is located.

E.g. on our DLAG- CD `x:\drivers\network\intel`

### **4.1.5 Driver installation WINDOWS 2000**

- Update the driver from the Intel® PRO/10+PCI device in the device manager.
- Choose the option "select list with drivers".
- Choose the "Intel 8255xx based Ethernet PCI Adapter(10/100)".
- Go on.

### **4.1.6 EEPROM update**

***Do not use this function, if the EEPROM is not corrupted !***

To download the data into the EEPROM, make the following steps:

- start MSDOS
- change into the directory: `c:\lan100\utility\ee2prom\...`
- type the following string: **`eeupdate -all lan100.eep lan100.dat`**

Now the EEPROM is updated again.

## 4.2 LAN Boot option *(since Version 1.4)*

The MSME104+ product is provided with an on-board FLASH ROM. The content of this ROM consists in a so-called BIOS extension, which enables your main board to be booted from LAN using the MSME104+ peripheral board.

The following section describes the procedure and different BIOS setup for the MSME104+ with the boot from LAN feature.

### 4.2.1 Setting up the system

Booting up the system with the pre-programmed FLASH ROM inserted (which already contains the Boot Agent Software from INTEL), you should obtain the following message after the POST routine has been completed.

Initializing Intel ® Boot Agent Version 4.0.00  
PXE m.m Build nnn (WfM w.w), RPL Vm.mm

Press Ctrl+S to enter the Setup Menu

To customize your Boot Agent Software, you can enter the setup, which allows you to set the following configuration values:

<b>Network Boot Protocol</b>		
	<i>PXE</i>	For use with WfM compatible network management programs, such as Intel LANDesk Mangement Suite, Windows 2000 RIS and Linux
	<i>RPL</i>	For legacy-style remote booting
<b>Boot Order</b>		Allows you to select the boot devices order on your computer
	<i>Use BIOS Setup Boot Order</i>	If your client does not support BBS or PnP compliant devices, this option will not be present
	<i>Try network first, then local drives</i>	
	<i>Try local drives first, then network</i>	
	<i>Try network only</i>	
	<i>Try local drives only</i>	
<b>Show Setup Prompt</b>		
	<i>Enable</i>	The Ctrl+S prompt will appear selecting this option
	<i>Disable</i>	The Ctrl+S prompt will not appear selecting this option
<b>Setup Menu</b>		Adjust the number of seconds the Boot Agent waits for someone to press Ctrl+S
	<i>0 seconds</i>	
	<i>2 seconds</i>	
	<i>3 seconds</i>	
	<i>4 seconds</i>	

<b>Legacy OS Wakeup Support</b>		Setting applies only to Intel PRO/100+WfM-compatible, 82559-based adapters
	<i>Enable</i>	Enable allows non-Windows operating systems (such as DOS) to use WfM-compatible adapter's remote wakeup capability
	<i>Disable</i>	Disable this setting using an ACPI Windows operating system (WIN98SE, WIN2000)

Note: It is possible to configure the Boot Agent in a Windows Environment (please refer to the [Intel Boot Agent User's Guide](#) available on the INTEL- homepage).

#### **4.2.2 Caution writing to the FLASH ROM**

Do only update the Boot Agent Software, if the content of the FLASH has been damaged or even lost. Using the fboot utility, you may experience problem with the FLASH update procedure ending with a failure.

With the SST 29 LE512 FLASH, the fboot utility always prompts the following message:

*flash write failure.*

If you are prompted with such a message, you should control if your FLASH device has been programmed to 100%. Then, reboot your system and the Boot Agent Software setup (as described in chapter 4.2.1) should normally be displayed.

If no setup is prompted or you can not boot from the network, repeat the procedure described in 4.2.3.

### **4.2.3 Updating the Flash ROM**

It is possible to program the on-board FLASH with the LAN BIOS extension using the *fboot* utility from Intel. Using the *fboot* program in a DOS environment, you should obtain the following message:

```
NIC      Network Address      PWA Number  Flash Memory      Size  Valid
===      =====
1        EEPROM Nr           XXXXXX-XXX  SST 29LE512      64    Yes
```

Select NIC to update or ESC to exit:

If more than one compatible adapter is installed in your system, you should obtain one after the other adapter to update. If you select 1, the following message will be prompted:

Select Option (U)pdate or (R)estore

This choice allows you to update the FLASH ROM with the Boot Agent Software (U), but also to (R)estore if you want to write store the file which the flash ROM was previously programmed with. This file should be present on your floppy or HD with an .FLS extension.

If you select (U) to update the FLASH, you will be prompted with the following message.

Create Restore Image? (Y)es or (N)o:

If you want to create a restore image of the FLASH ROM not yet updated, choose (Y)es, else type (N)o. Typing (Y)es, a backup file of the FLASH content (named xxxxxxxx.fls with xxxxxxxx being the last eight digits of the adapter's Ethernet address) is created. The following message is then displayed:

Continue Update without restore image? (Y)es or (N)o:

Typing (Y)es, the FLASH ROM will be updated. A current version of the Boot Agent Software will be written in the FLASH ROM. This process should last less than 10 seconds and the *fboot* procedure should end with the DOS prompt. If you type (N)o, the content is leaved unchanged and the update is cancelled.

### **4.2.4 Useful addresses**

Working with the MSME104+ peripheral board, you could need some information regarding the Intel Boot Agent software. This information can be found at the following addresses:

<http://support.intel.com>

<http://www.intel.com/network>

<http://developer.intel.com>

### 4.3 SCSI Interface (option)

**Please note, that the option SCSI-2 is not available on the SCSI connector J3, as these additional data signals are not connected to this connector.**

The SCSI-2 interface is realized with the AIC-7880 controller. This chip is fully supported by Adaptec Device Management System (SDMS) software, that supports the Advanced SCSI Protocol Interface (ASPI) and the ANSI Common Access Method (CAM). The AIC-7880 operates the SCSI bus at 5 MB/s asynchronously or 10 MB/s synchronously, and bursts data to the host at full PCI speed up to 110 MB/s (at 33 MHz).

The SCSI-2 controller has full PnP recognition, a 64-Byte DMA FIFO and all SCSI signals are ESD protected up to 2 kV.

The user can connect up to 7 SCSI devices to the AIC-7880, all the SCSI devices are daisy chained through one SCSI-Bus cable. This cable must have terminators at both ends; i.e. the beginning device and end device.

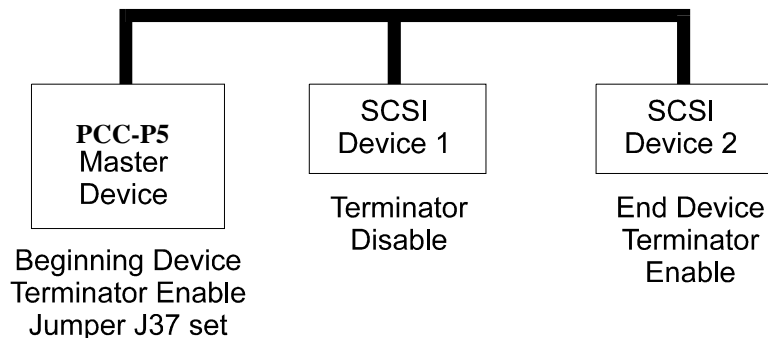
Without proper installation of the terminators it will cause a SCSI devices malfunction.

On the e.g. PCC-P5L board, the terminator is active, when jumper J102 is set to 1-2.

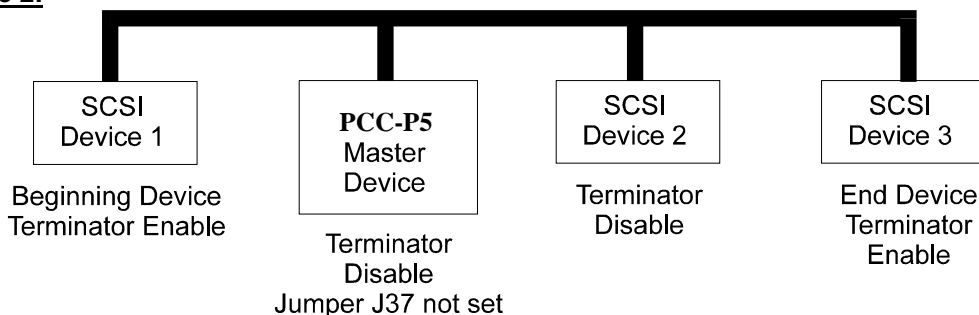
On position 2-3 the termination will be auto detected.

The following figures illustrate, where the terminators can be placed:

#### Example 1:



#### Example 2:



#### The boot devices on the SCSI-2 interface:

- Any SCSI-2 harddisk
- Syquest removable media
- CD drives
- Tapes, MO- and ZIP-Drives

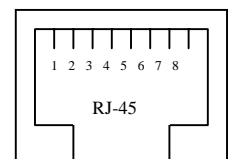
## 5 CONNECTORS ON THE BOARD

### J3 SCSI connector, (no SCSI-2 available)

Pin	Signal	Pin	Signal
Pin 2	SCSI data 0	Pin 1	GND
Pin 4	SCSI data 1	Pin 3	GND
Pin 6	SCSI data 2	Pin 5	GND
Pin 8	SCSI data 3	Pin 7	GND
Pin 10	SCSI data 4	Pin 9	GND
Pin 12	SCSI data 5	Pin 11	GND
Pin 14	SCSI data 6	Pin 13	GND
Pin 16	SCSI data 7	Pin 15	GND
Pin 18	SCSI parity	Pin 17	GND
Pin 20	GND	Pin 19	GND
Pin 22	Terminator	Pin 21	GND
Pin 24	GND	Pin 23	GND
Pin 26	Terminator power	Pin 25	GND
Pin 28	GND	Pin 27	GND
Pin 30	GND	Pin 29	GND
Pin 32	SCSI ATN	Pin 31	GND
Pin 34	GND	Pin 33	GND
Pin 36	SCSI BUSY	Pin 35	GND
Pin 38	SCSI ACK	Pin 37	GND
Pin 40	SCSI Reset	Pin 39	GND
Pin 42	SCSI MSG	Pin 41	GND
Pin 44	SCSI Select	Pin 43	GND
Pin 46	SCSI CD	Pin 45	GND
Pin 48	SCSI REQ	Pin 47	GND
Pin 50	SCSI IO	Pin 49	GND

### J2 Ethernet Twisted Pair interface 10/100Mhz

	RJ-45 Pin	Signal
	Pin 1	= TX+
	Pin 2	= TX-
	Pin 3	= RX+
	Pin 6	= RX-
	Pin 4,5,7,8	Pulled down with 75ohms



\* This signals are ready to connect directly to a RJ-45 connector.

**J1** PC/104+ BUS interface

Pin	A	B	C	D
1	GND/5.0V KEY2	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY2

## Notes:

1. The shaded area denotes power or ground signals.
2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding..

**J5** **PC/104 BUS interface, only as carrier connector for stack through options**

Pin	A:	B:	C:	D:
0			Ground	Ground
1	IOCHCK	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	+5V	LA22	IRQ10, (redirected)
4	SD5	(IRQ9), (redirected)	LA21	IRQ11, (redirected)
5	SD4	(-5V)	LA20	IRQ12, (PIRQ2)
6	SD3	DRQ2	LA19	IRQ15, (redirected)
7	SD2	(-12V)	LA18	IRQ14, (PIRQ0)
8	SD1	(SRDY)	LA17	(DACK0)
9	SD0	+12V	MEMR	DRQ0
10	IOCHRDY	Ground	MEMW	(DACK5)
11	AEN	SMEMW	SD8	(DRQ5)
12	SA19	SMEMR	SD9	(DACK6)
13	SA18	SIOW	SD10	(DRQ6)
14	SA17	SIOR	SD11	(DACK7)
15	SA16	(DACK3)	SD12	(DRQ7)
16	SA15	(DRQ3)	SD13	+5 Volt
17	SA14	DACK1	SD14	MASTER
18	SA13	DRQ1	SD15	Ground
19	SA12	REF	Ground	Ground
20	SA11	SYSCLK		
21	SA10	IRQ7 (PIRQ7)		
22	SA9	IRQ6 (PIRQ6)		
23	SA8	IRQ5 (PIRQ5)		
24	SA7	IRQ4 (PIRQ4)		
25	SA6	IRQ3 (PIRQ3)		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5 Volt		
30	SA1	OSC		
31	SA0	Ground		
32	Ground	Ground		

## **6 JUMPER DESCRIPTION**

### **6.1 The jumpers for the SCSI circuit on this product**

<b>J10 PCI-Bus Clock Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>PCICLK 0</b>
3-4	none	PCICLK 1
5-6	none	PCICLK 2
7-8	none	PCICLK 3

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J11 PCI-IDSEL Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>ID 0</b>
3-4	none	ID 1
5-6	none	ID 2
7-8	none	ID 3

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J13 PCI-IRQ Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>IRQ A</b>
3-4	none	IRQ B
5-6	none	IRQ C
7-8	none	IRQ D

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J12 PCI-REQUEST Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>REQ 0</b>
3-4	none	REQ 1
5-6	none	REQ 2
7-8	none	REQ 3

Only one of this selection may be closed. Use a signal, which is from no other board used. The GRANT and the REQ number must be on the same number.

<b>J12 PCI-GRANT Source</b>	<b>open</b>	<b>closed</b>
9-10	none	<b>GNT 0</b>
11-12	none	GNT 1
13-14	none	GNT 2
15-16	none	GNT 3

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J17 Flash Address Set</b>	<b>open</b>	<b>closed</b>
	A16	<b>A16=0</b>

<b>J18 Flash Address Set</b>	<b>open</b>	<b>closed</b>
	A17	<b>A17=0</b>

<b>J15 Flash VP select</b>	<b>1-2</b>	<b>2-3</b>
	VP=3,3V	<b>VP to GND</b>

The SCSI device does not require to write to the FLASH ROM.

<b>J16 Flash VCC select</b>	<b>1-2</b>	<b>2-3</b>
	<b>VCC=5V</b>	VCC=3.3V

<b>J14 Vcc 3.3V select</b>	<b>open</b>	<b>closed</b>
	<b>From PC104+</b>	internal

(Optional, not assembled)

<b>J4 SCSI termination</b>	<b>1-2</b>	<b>2-3</b>
	<b>enabled</b>	disabled

**Setting written in bold are default !**

## **6.2 The jumpers for the LAN100 circuit on this product**

<b>J6 PCI-Bus Clock Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>PCICLK 0</b>
3-4	none	PCICLK 1
5-6	none	PCICLK 2
7-8	none	PCICLK 3

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J7 PCI-IDSEL Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>ID 0</b>
3-4	none	ID 1
5-6	none	ID 2
7-8	none	ID 3

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J9 PCI-IRQ Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>IRQ A</b>
3-4	none	IRQ B
5-6	none	IRQ C
7-8	none	IRQ D

Only one of this selection may be closed. Use a signal, which is from no other board used.

<b>J8 PCI-REQUEST Source</b>	<b>open</b>	<b>closed</b>
1-2	none	<b>REQ 0</b>
3-4	none	REQ 1
5-6	none	REQ 2
7-8	none	REQ 3

Only one of this selection may be closed. Use a signal, which is from no other board used. The GRANT and the REQ number must be on the same number.

<b>J8 PCI-GRANT Source</b>	<b>open</b>	<b>closed</b>
9-10	none	<b>GNT 0</b>
11-12	none	GNT 1
13-14	none	GNT 2
15-16	none	GNT 3

Only one of this selection may be closed. Use a signal, which is from no other board used. The GRANT and the REQ number must be on the same number!

<b>J17 Flash Address Set</b>	<b>open</b>	<b>closed</b>
	<b>A16</b>	A16=0

<b>J18 Flash Address Set</b>	<b>open</b>	<b>closed</b>
	<b>A17</b>	A17=0

J15 Flash VP select	1-2	2-3
	<b>VP=3,3V</b>	VP to GND

J15 is set to 1-2 to enable the fboot utility (refer to section 4.2.2) to write to the FLASH.

J16 Flash VCC select	1-2	2-3
	VCC=5V	<b>VCC=3.3V</b>

J14 Vcc 3.3V select	open	closed
	<b>From PC104+</b>	internal

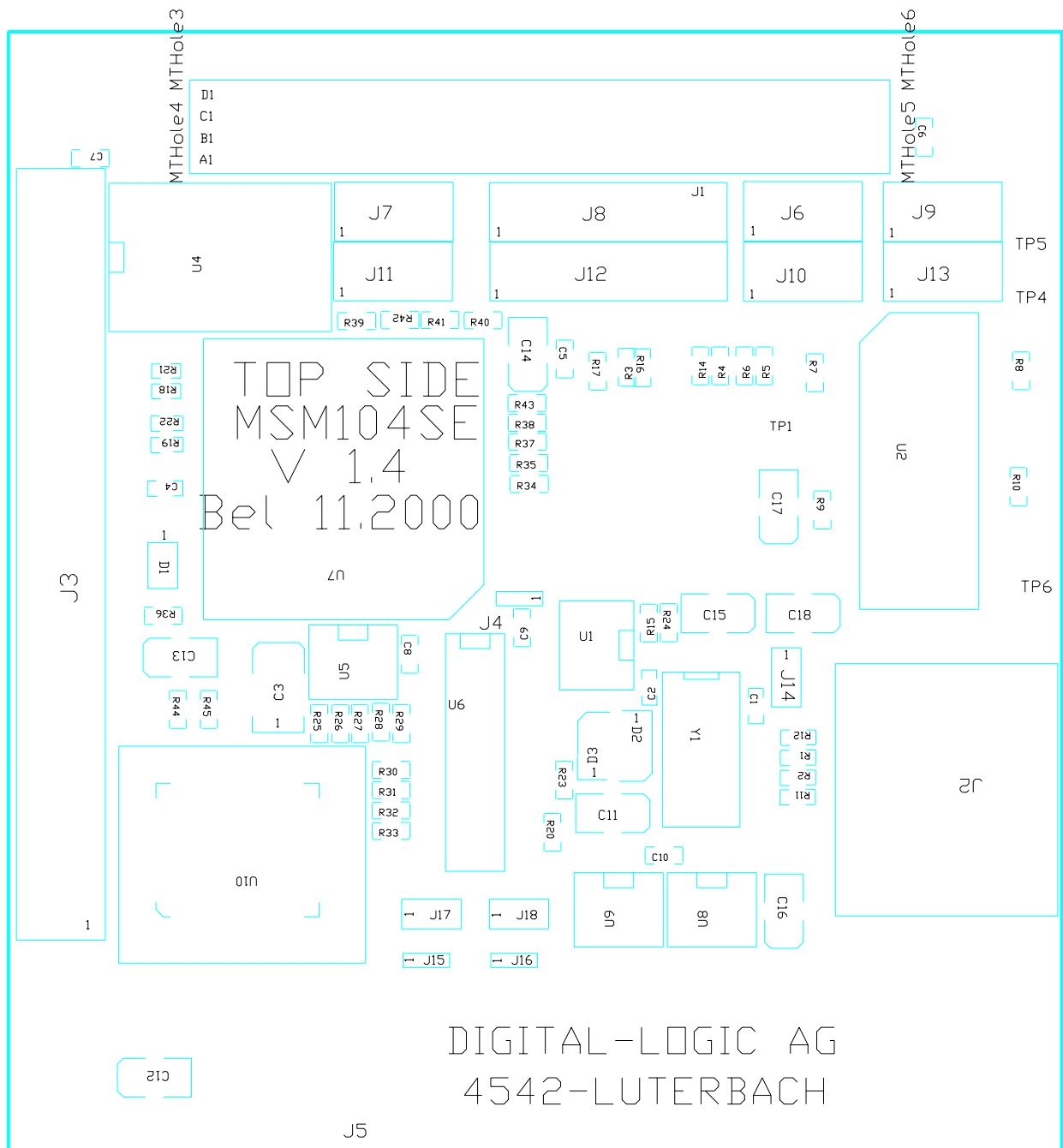
(Optional, not assembled)

Setting written in bold are default !

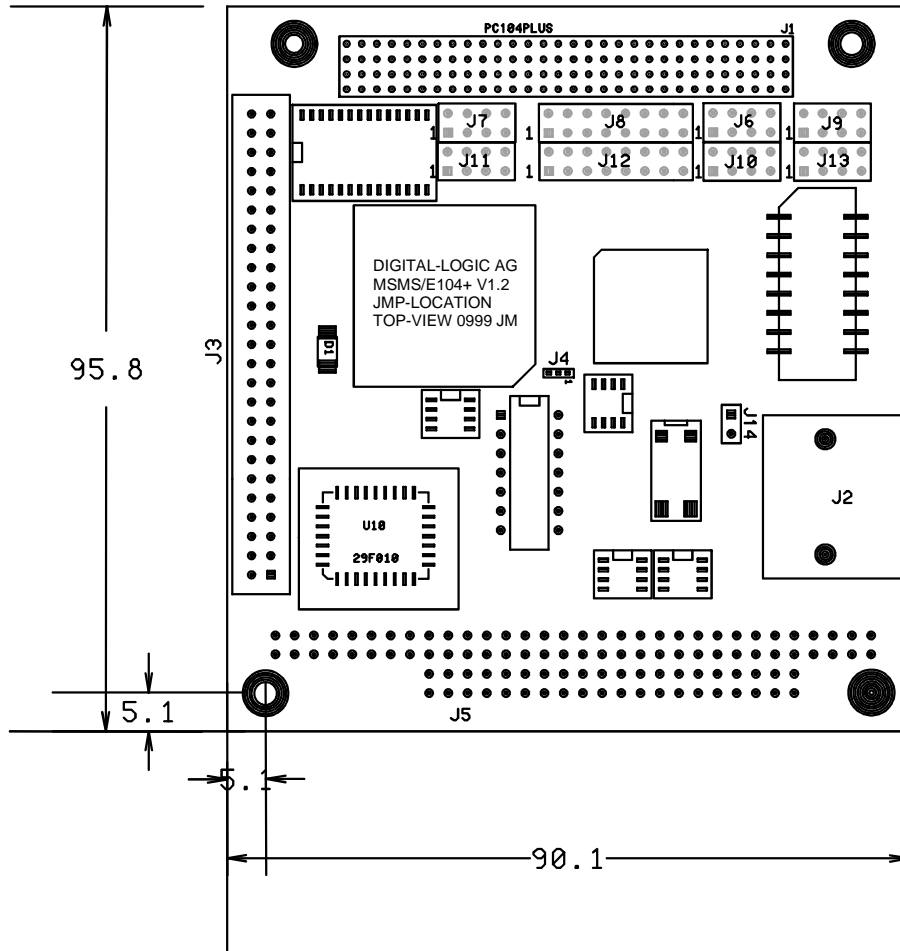
## 7 LED CRITERIONS:

LED	Color	Function
D3	red	SCSI activity

**7.1 Jumper- and part locations of the MSMS/E104+, V1.4**



**7.2 Main dimensions of the board, version V1.2**



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