

CPUBoard

EBC 363 Series

User's Manual

This manual serves all EBC363 series

3.5" Pentium®III/Celeron™ class Low Power Embedded Controller w/CPU/Video/LAN/Audio/1394/TVout

● **Introduction**

EBC 363 is a compact powerful 3.5" Pentium®III/ Celeron™ class low power embedded controller. The board is built on VIA C3 EBGA CPU **800MHz+** at 100/133MHz FSB, with VIA 8606/686B (Twister T) core logic chipset. The EBC 363 features VIA 8606, which support 3D graphics and LVDS/TTL LCD interface, one RTL 8139C full duplex Ethernet Controller, TV output, on board IEEE 1394 and on-board Audio. Besides, for expandability, EBC 363 offers PC 104 socket for future expansion.

● **Features**

- VIA C3 EBGA CPU 800MHz+ on board, VIA C3 series CPU with EBGA Package at FSB 100/133MHz FSB
- CPU fan-less support up to 400MHz
- Max. 512MB SDRAM, DIMM x1
- VIA Twister 8606/686B chipsets w/ 4x AGP VGA built-in
- 3D graphic, LVDS (18bit x 2)/TTL LCD interface (24bit x 1)
- Realtek 8139C/C+ 10/100 Base T/TX LAN
- AC 97 ver. 2.0 Audio
- TV output/IEEE 1394/USB

● **Specifications**



System Architecture

- 3.5" small form factor with Dimensions: **143 x 102 mm**
- On board VIA C3 Processor EBGA package with **128KB** Level 1 and 64 KB level 2 cache
- FSB 100/133MHz



CPU support

- Onboard VIA C3 Processor EBGA Package with **128KB** Level 1 and 64KB Level 2 Cache
- 800MHz+ CPU on board by CPU FSB 100/133MHz
- **Ultra Low Power CPU Fan-less feature at CPU speed 400MHz up to 667MHZ in the future**



Memory

- One 144-pin SO-DIMM. Support Max memory size to 512MB



BIOS

- Award system BIOS
- Optional ACPI Support
- Advanced power management support
- 4M bits flash ROM



Chipset

- VIA 8606 (Twister T) 100 /133 MHz North Bridge
- VIA VT82C686B PCI SUPER-I/O integrated peripheral controller



On board LAN

- RealTek RTL8139C/C+ Ethernet Controller x1
- Single Chip 10 /100 Base TX support, full duplex
- Compliant with IEEE802.3X
- Boot from LAN function
- Drivers support: DOS/Windows® Windows®95/98/2000, Windows®NT, Netware, SCO Open Server 5.0, Linux 7.2 or later, FreeBSD
- RJ45 with LED connector x1



On Board Audio

- VT82C686B and AC97 ver. 2.0 compliant interface, Multi-stream Direct Sound and Direct Sound 3D acceleration
- Audio interface:
CD audio in, Line in (Internal connector)
Microphone in, Speaker out (with Amplifier)



On Board VGA

- VIA 8606 Integrated Savage4 2D/3D/Video Accelerator
 - Optimized Shared Memory Architecture (SMA)
 - 8/16/32MB frame buffer using system memory
 - Single cycle 128-bit 3D architecture
 - Full internal AGP 4x performance
 - Next generation, 128-bit 2D graphics engine
 - High quality DVD video playback
 - 2D/3D resolutions up to 1920x1440
 - 3D Rendering Features

- Extensive LCD Support
 - 36-bit TFT flat panel interface with 256 gray shade support
 - Integrated 110 MHz LVDS interface (18bit x 2)
 - Support for all resolutions up to 1600x1200
 - Drivers support: Windows®95/98/2000, Windows®NT4.0, Linux
 - 15Pin D-Sub VGA Output
 - LVDS Interface Connector **x 2**
 - TTL LCD Interface Connector x1
- **On Board External TV Encoder Interface**
- TV encoder
 - **RCA TV out & S-Video output**
 - Supports NTSC, NTSC-EIA (Japan) and PAL TV formats
- **On Board IEEE1394**
- VIA Fire II VT6306
 - IEEE 1394-1394A compliant
 - OHCI compatible programming interface
 - 100/200/400 Mbps data transfer rates
 - PCI 2.1 interface
 - 1394 Port x3 (one direct output, 2 port by Pin Header reserved)
- **On Board IDE Interface**
- VIA 686B South Bridge Integrated UltraDMA-33/66/100 master mode EIDE controller
 - Support UltraDMA -33/66/100 IDE with 44 pin connector ×1 (primary)
 - Internal Compact Flash socket x 1 (secondary)
- **On Board Bus Expansion**
- **NEXCOM PCI Proprietary Connector for PCI devices**
 - PC/104 connector: One 16-bit 104-pin connector onboard
- **Dimensions**
- 143mm(L) × 102mm(W)

➤ **On Chip and On board I/O**

- SIO× 2, with 4x16C550 UARTs, 10 pin header (2.0mm) ×2 ; one for RS422/485
- PIO× 1, bi-directional, EPP/ECP support, 26 pin connector ×1
- 6 pin mini DIN connector ×1, for PS/2 keyboard/mouse
- On board USB port ×2
- On Board buzzer ×1
- Digital I/O TTL level (4 in 4 out)
- On board 3 pin header for I²C, one pin for GND;
- On board 5 pin header for IrDA Tx Rx
- On Board 2 pin header for Reset SW
- On Board 2 pin header for power SW (ATX Mode)
- On Board 2 pin Power LED Header
- 2 pin Power Header x1 for Panel (5V or 3.3V)
- 3 pin Power Connector x2 for CPU FAN and Chassis FAN
- 2 Pin IDE Active LED Header

➤ **Real Time Clocker**

- On chip RTC with battery back up
- External Li Battery x1

➤ **Watchdog Timer**

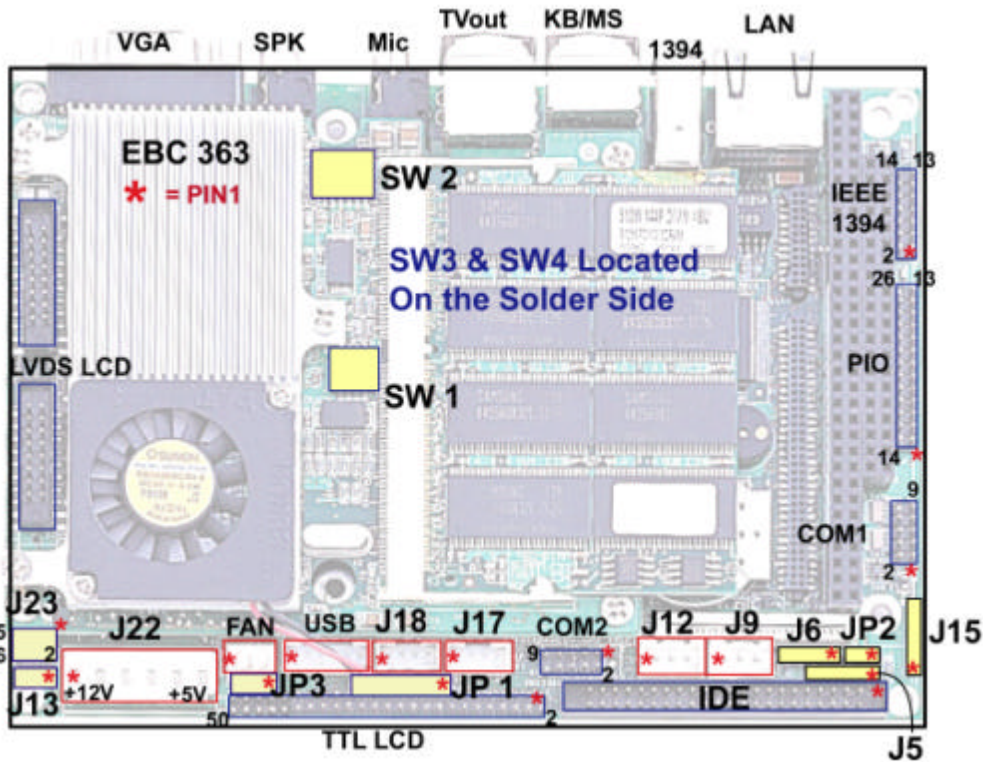
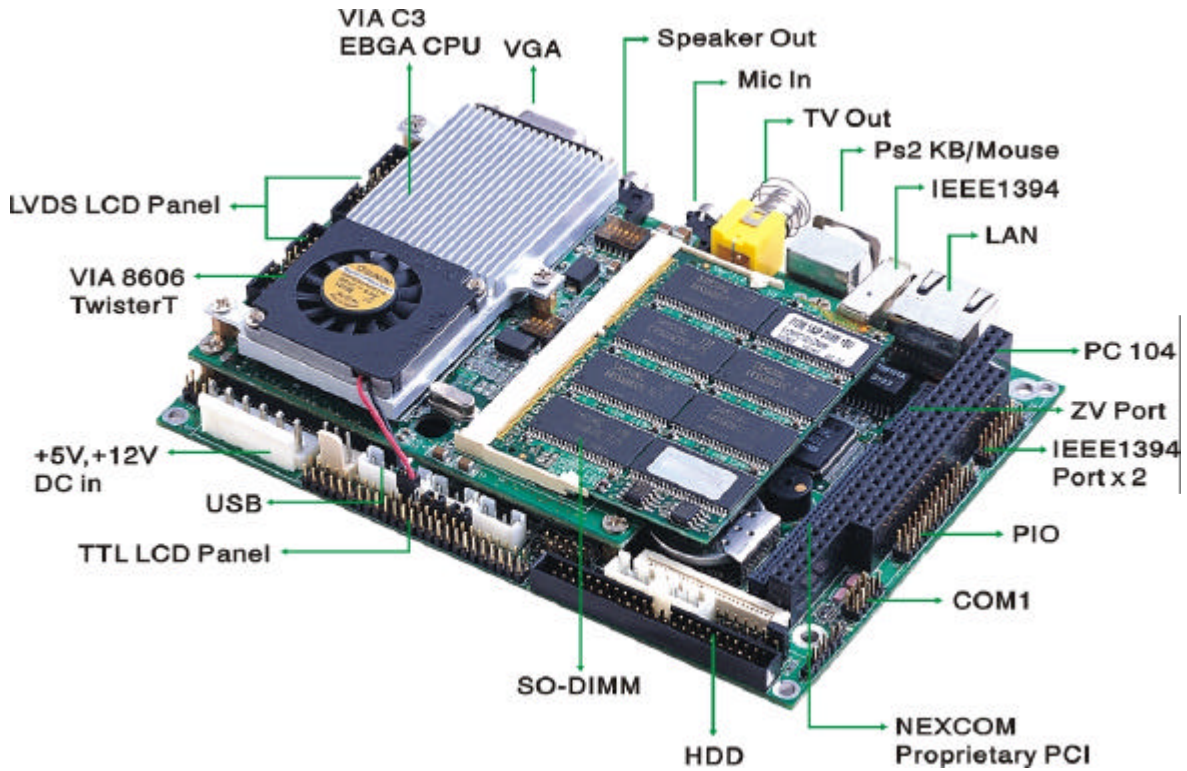
- Watchdog timeout can be programmable by Software

➤ **System Monitor**

- Derived from Super IO to support system monitor
- 5 voltage (For +3.3V, +5V, +5Vsb, +12V, Vcore)
- Fan speed For CPU
- Temperature
- Drivers support: Windows®95/98/2000, Windows NT4.0

Chapter 2

Switches and Connectors



EBC363 Pin Definition :

Connector On CPU Module:

- J1: Primary LVDS Panel Interface / J2: Secondary LVDS Panel Interface

Pin No.	Definition	Pin No.	Definition
1.	LVDS Data 2 Positive Output.	2.	LVDS Data 2 Negative Output.
3.	GND.	4.	GND.
5.	LVDS Data 1 Positive Output.	6.	LVDS Data 1 Negative Output.
7.	GND.	8.	GND.
9.	LVDS Data 0 Positive Output.	10.	LVDS Data 0 Negative Output.
11.	GND.	12.	GND.
13.	LVDS Click Positive Output.	14.	LVDS Clock Negative Output.
15.	Panel Power(5V or 3.3V).	16.	Panel Power (5V or 3.3V).

Connector On I/O Board :

- J15:

Pin No.	Definition
1.	Power button.
2.	GND. (for Power button.)
3.	Reset Switch.
4.	GND. (for Reset Switch.)
5.	IRQ7 Input.
6.	WDT Time Out Output.(When Signal High Means WDT was time out.)

- J24: COM1 (RS232 Port)

Pin No.	Definition	Pin No.	Definition
1.	DCD#: Data Carrier Detect.	2.	RXD#: Receive Data.
3.	TXD: Transmit Data.	4.	DTR#: Data Terminal Ready.
5.	GND.	6.	DSR#: Data Set Ready.
7.	RTS#: Request To Send.	8.	CTS#: Clear To send.
9.	RI#: Ring Indicator.		

- J14: COM2 (RS232 Mode: When SW3.2~SW3.7 (SW3 on I/O board.) Off ,
and JP1 Pin4, Pin5 Short
RS422 Mode: When SW3.2 Off, SW3.3 On, SW3.4~SW3.7 On,
and JP1 Pin4, Pin5 Short
RS485 Mode: When SW3.2 On, SW3.3 Off, SW3.4~SW3.7 On.)

- *RS232 Mode:*

Pin No.	Definition	Pin No.	Definition
1.	DCD#: Data Carrier Detect.	2.	RXD#: Receive Data.
3.	TXD: Transmit Data.	4.	DTR#: Data Terminal Ready.
5.	GND.	6.	DSR#: Data Set Ready.
7.	RTS#: Request To Send.	8.	CTS#: Clear To send.
9.	RI#: Ring Indicator. (Could be a 5V or 12V Power Pin.)		

- *RS422 Mode:*

Pin No.	Definition	Pin No.	Definition
1.	TXD-: Transmit Data Negative.	2.	TXD+: Transmit Data Positive.
3.	RXD+: Receive Data Positive.	4.	RXD-: Receive Data Negative.
5.	GND. DCD#: Data Carrier Detect.	6.	RTS-: Request To Send Negative .
7.	RTS+: Request To Send Positive .	8.	CTS+: Clear To send Positive.
9.	CTS-: Clear To send Negative. (Could be a 5V or 12V Power Pin.)		

- *RS485 Mode:*

Pin No.	Definition	Pin No.	Definition
1.	TXD-: Transmit Data Negative. / RXD-: Receive Data Negative.	2.	TXD+: Transmit Data Positive. / RXD+: Receive Data Positive.
3.	Reserved.	4.	Reserved.
5.	Reserved.	6.	Reserved.
7.	Reserved.	8.	Reserved.
9.	Reserved. (Could be a 5V or 12V Power Pin.)		

Note : When JP1 Pin 4, Pin5 Short Then J14 Pin9 set as normal function.

When JP1 Pin 5, Pin6 Short and JP1 Pin 1, Pin 2 Short then J14 Pin9 set as 5V Power Pin.

When JP1 Pin 5, Pin6 Short and JP1 Pin 2, Pin 3 Short then J14 Pin9 set as 12V Power Pin.

- J19: Parallel Port.

Pin No.	Definition	Pin No.	Definition
1.	Strobe#.	14.	Auto Feed.
2.	Parallel Port Data 0.	15.	Error.
3.	Parallel Port Data 1.	16.	Initialize#.
4.	Parallel Port Data 2.	17.	Select In#.
5.	Parallel Port Data 3.	18.	GND
6.	Parallel Port Data 4.	19.	GND
7.	Parallel Port Data 5.	20.	GND
8.	Parallel Port Data 6.	21.	GND
9.	Parallel Port Data 7.	22.	GND
10.	Acknowledge#.	23.	GND
11.	Busy#.	24.	GND
12.	Paper End	25.	GND
13.	Select		

- J3: IEEE 1394 Port.

Pin No.	Definition.	Pin No.	Definition.
1.	Port 1 Twisted Pair A Positive.	2.	Port 1 Twisted Pair A Negative.
3.	GND.	4.	Port 1 Twisted Pair B Negative.
5.	Port 1 Twisted Pair B Positive.	6.	IEE1394 Port 1 Power Output.
7.	Port 2 Twisted Pair A Positive.	8.	Port 2 Twisted Pair A Negative.
9.	GND.	10.	Port 2 Twisted Pair B Negative.
11.	Port 2 Twisted Pair B Positive.	12.	IEE1394 Port 2 Power Output.
13.	GND.		

- J5: General Purpose I/O Port.

Pin No.	Definition
1.	Power Output. <i>Note.</i>
2.	GND.
3.	GP I/O A.
4.	GP I/O B.
5.	GP I/O C.
6.	GP I/O D.

Note: When JP1 Pin1 and Pin2 is short then J5 Pin1 Output 5V.

When JP1 Pin2 and Pin3 is short then J5 Pin1 Output 12V.

- IDE1: Primary Ultra DMA-33/66/100 Enhanced IDE Interface

Pin No.	Definition	Pin No	Definition
1.	Reset #	2.	GND.
3.	Disk Data 7.	4.	Disk Data 8.
5.	Disk Data 6.	6.	Disk Data 9.
7.	Disk Data 5.	8.	Disk Data 10.
9.	Disk Data 4.	10.	Disk Data 11.
11.	Disk Data 3.	12.	Disk Data 12.
13.	Disk Data 2.	14.	Disk Data 13.
15.	Disk Data 1.	16.	Disk Data 14.
17.	Disk Data 0.	18.	Disk Data 15.
19.	GND.	20.	NC
21.	Device DMA Request.	22.	GND.
23.	Device I/O Write.	24.	GND.
25.	Device I/O Read.	26.	GND.
27.	I/O Channel Ready.	28.	Pull Down to GND.
29.	Device DMA Acknowledge.	30.	GND.
31.	Interrupt.	32.	NC.
33.	Disk Address 1.	34.	ATA 66/100 Cable select.
35.	Disk Address 0.	36.	Disk Address 2.
37.	Master Chip Select.	38.	Slave Chip Select.
39.	Hard Disk LED.	40.	GND.
41.	5V Power Output.	42.	5V Power Output.
43.	GND.	44.	NC.

- J6: Infrared Interface.

Pin No.	Definition
1.	5V Power Output.
2.	NC.
3.	Infrared Receive.
4.	GND.
5.	Infrared Transmit.

- J9: -12V/-5V Input Connector reserve for PC104 add on card.

Pin No.	Definition
1.	GND.
2.	-5V Input.
3.	-12V Input.

- J12: ATX Power Function Connector.

Pin No.	Definition
1.	Standby 5V Input.
2.	GND.
3.	ATX Power, Power On

- J8: Note Book type FDD Connector.

Pin No.	Definition	Pin No.	Definition
1.	5V Power Output.	2.	INDEX#.
3.	5V Power Output.	4.	DS0#.
5.	5V Power Output.	6.	DSKCHG#.
7.	NC.	8.	NC.
9.	NC.	10.	MTR0#.
11.	NC.	12.	DIR#.
13.	DRVDEN0.	14.	STEP#.
15.	GND.	16.	WDATA#.
17.	GND.	18.	WGATE#.
19.	GND.	20.	TRK0#.
21.	GND.	22.	WRTPRT#.
23.	GND.	24.	RDATA#.
25.	GND.	26.	HDSEL#.

- JP1: Expand Power Output Pin.

Pin No.	Definition
7.	Power Output. <i>Note.</i>
8.	GND.

Note: When JP1 Pin1 and Pin2 is short then J5 Pin1 Output 5V.

When JP1 Pin2 and Pin3 is short then J5 Pin1 Output 12V

- FAN1: CPU FAN Connector.

Pin No.	Definition
1.	GND.
2.	Power Output. Note
3.	FAN Detect.

Note: When JP3 Pin1/Pin2 short, then FAN1 Pin2 output +12V Power.

When JP3 Pin2Pin3 short, then FAN1 Pin2 output +5V Power.

CN3: Panel interface.

Pin No.	Definition	Pin No.	Definition
		2.	12V Safe.
3.	FPHS.	4.	FPDEN.
5.	FPCLK.	6.	FPVS.
7.	FPD25.	8.	VDD Safe.
9.	FPD24.	10.	FPD31.
11.	FPD28.	12.	FPD26.
13.	FPD32.	14.	FPD30.
15.	FPD13.	16.	FPD34.
17.	FPD12.	18.	FPD19.
19.	FPD16.	20.	VDD Safe.
21.	FPD20.	22.	FPD14.
23.	GND.	24.	FPD18.
25.	FPD1.	26.	FPD22.
27.	FPD0.	28.	FPD7.
29.	FPD4.	30.	Backlight enabled
31.	FPD8.	32.	FPD2.
33.	GND.	34.	FPD6.
35.	FPD3.	36.	FPD10.
37.	FPD9.	38.	FPD5.
39.	FPCLK.	40.	GND.
41.	FPD15.	42.	FPD11.
43.	FPD21.	44.	FPD17.
45.	FPD27.	46.	FPD23.
47.	FPD33.	48.	FPD29.
49.	GND.	50.	FPD35.

Mapping Table

Pin Name	TFT18	TFT2x18	TFT24
FPD0	R0	R00	R2
FPD1		R10	R0
FPD2	R1	R01	R3
FPD3		R11	
FPD4	R2	R02	R4
FPD5		R12	
FPD6	R3	R03	R5
FPD7		R13	R1
FPD8	R4	R04	R6
FPD9		R14	
FPD10	R5	R05	R7
FPD11		R15	
FPD12	G0	G00	G2
FPD13		G10	G0
FPD14	G1	G01	R3
FPD15		G11	
FPD16	G2	G02	G4
FPD17		G12	
FPD18	G3	G03	G5
FPD19		G13	G1
FPD20	G4	G04	G6
FPD21		G14	
FPD22	G5	G05	G7
FPD23		G15	
FPD24	B0	B00	B2
FPD25		B10	B0
FPD26	B1	B01	B3
FPD27		B11	
FPD28	B2	B02	B4
FPD29		B12	
FPD30	B3	B03	B5
FPD31		B13	B1
FPD32	B4	B04	B6
FPD33		B14	
FPD34	B5	B05	B7
FPD35		B15	

- J23: LED

Pin No.	Definition	Pin No.	Definition
1.	Power For Suspend LED	2.	Suspend LED
3.	+5V(Standby 5V) LED	4.	GND for +5V (Standby 5V) LED
5.	Power For HDD LED	6.	HDD LED

- J17: Audio / Line In

Pin No.	Definition
1.	Line In Right.
2.	GND.
3.	GND.
4.	Line In Left.

- J18: Audio / CD In

Pin No.	Definition
1.	CD In Left.
2.	GND.
3.	GND.
4.	CD In Right.

- USB1: USB Interface.

Pin No.	Definition
1.	5V Power Output.
2.	USB Port 0 Data-
3.	USB Port 0 Data+
4.	USB Port 1 Data-
5.	USB Port 1 Data+
6.	GND.

- J22: Main Power Input Connector.

Pin No.	Definition
1.	12V Power Input
2.	GND.
3.	GND.
4.	GND.
5.	5V Power Input.
6.	5V Power Input.

- J13: SM Bus

Pin No.	Definition
1.	SM Bus Clock
2.	SM Bus Data
3.	GND

EBC363 Jumper Setting

Switch On CPU Module

SW1: For Panel Type.

SW1.4	SW1.3	SW1.2	SW1.1	BIOS Setup	Function
On	On	On	On	00	640x480 TFT
On	Off	On	On	01	800x600 TFT
Off	On	On	On	02	1024x768 TFT 2pixel/clock at 32Mhz (LVDS)
Off	Off	On	On	03	1280x1024 TFT
On	On	Off	On	04	640x480 DSTN
On	Off	Off	On	05	800x600 DSTN
Off	On	Off	On	06	1024x768 DSTN
Off	Off	Off	On	07	1024x768 TFT 1pixel/clock at 65Mhz (LVDS)
On	On	On	Off	08	640x480 TFT
On	Off	On	Off	09	800x600 TFT
Off	On	On	Off	0A	1024x768 TFT
Off	Off	On	Off	0B	1280x1024 TFT
On	On	Off	Off	0C	1400x1050 TFT 2pixel/clock at 54Mhz (LVDS)
On	Off	Off	Off	0D	800x600 DSTN
Off	On	Off	Off	0E	1024x768 DSTN
Off	Off	Off	Off	0F	1280x1024 DSTN

SW2: CPU BUS Ratio. Only for 800MHz or higher frequency CPU

SW2.1	SW2.2	SW2.3	SW2.4	SW2.5	BUS Ratio
ON	ON	ON	ON	ON	9.0X
ON	ON	ON	ON	OFF	3.0X
ON	ON	ON	OFF	ON	4.0X
ON	ON	ON	OFF	OFF	10.0X
ON	ON	OFF	ON	ON	5.5X
ON	ON	OFF	ON	OFF	3.5X
ON	ON	OFF	OFF	ON	4.5X
ON	ON	OFF	OFF	OFF	9.5X
ON	OFF	ON	ON	ON	5.0X
ON	OFF	ON	ON	OFF	7.0X
ON	OFF	ON	OFF	ON	8.0X
ON	OFF	ON	OFF	OFF	6.0X
ON	OFF	OFF	ON	ON	12.0X
ON	OFF	OFF	ON	OFF	7.5X
ON	OFF	OFF	OFF	ON	8.5x
ON	OFF	OFF	OFF	OFF	6.5X
OFF	ON	ON	ON	ON	Reserved
OFF	ON	ON	ON	OFF	11.0X
OFF	ON	ON	OFF	ON	12.0X
OFF	ON	ON	OFF	OFF	Reserved
OFF	ON	OFF	ON	ON	13.5X
OFF	ON	OFF	ON	OFF	11.5X
OFF	ON	OFF	OFF	ON	12.5X
OFF	ON	OFF	OFF	OFF	10.5X
OFF	OFF	ON	ON	ON	13.0X
OFF	OFF	ON	ON	OFF	15.0X
OFF	OFF	ON	OFF	ON	16.0X
OFF	OFF	ON	OFF	OFF	14.0X
OFF	OFF	OFF	ON	ON	Reserved
OFF	OFF	OFF	ON	OFF	15.5X
OFF	OFF	OFF	OFF	ON	Reserved
OFF	OFF	OFF	OFF	OFF	14.5X

Switch And Jumper On I/O Board

- JP2: Panel Power Type.

Pin1 Short with Pin2	For 5V Panel.
Pin2 Short With Pin3	For 3.3V Panel.

- JP1: Power Type For JP1 Pin7 / J14 Pin 9 (If JP1 Pin5, Pin6 Short) / J5 Pin1.

Pin1 Short with Pin2	5V.
Pin2 short With Pin3	12V.

JP3: CPU FAN Voltage

PIN 1-2 Short	12V
PIN 2-3 Short	5V

- SW3.1: BIOS Flash-able.

SW3.1	Function
ON	Enable.
OFF	Disable.

- SW3.2~SW3.7: COM2 Mode (RS232/RS422/RS485).

SW3.2	SW3.3	SW3.4.	SW3.5	SW3.6	SW3.7	Function
OFF	OFF	OFF	OFF	OFF	OFF	RS232
OFF	ON	ON	ON	ON	ON	RS422
ON	OFF	ON	ON	ON	ON	RS485

- SW3.8, SW3.9: CMOS Data Clear.

SW3.8	SW3.9	Function
ON	OFF	Clear CMOS Data
OFF	ON	Normal

Note: Please, Don't turn on SW3.8 and SW3.9 at the same time that will reduce the battery lifetime.

- SW4.1, SW4.2: Mouse Data / IRQ12

SW4.1	SW4.2	Function
ON	OFF	When Enable Mouse, should switch to this type
OFF	ON	When Disable Mouse and switch to this type then IRQ12 will release for ISA BUS.

- SW4.3: Keyboard Power On

SW4.3	Function
ON	Enable
OFF	Disable

- SW4.4: LAN Enable

SW4.4	Function
OFF	Enable
ON	Disable

Award's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed RAM (CMOS RAM) so that it retains the Set up information when the power is turned off.

The Chapter shows the currently BIOS setup picture is for reference only, which may change by the BIOS modification in the future. Any Major updated items or re-version, user can download from NEXCOM web site <http://www.nexcom.com.tw> or any unclear message, can contact NEXCOM Customer Service people for help <http://www.nexcom.com.tw/contact/contact.htm>

✓ **Entering Setup**

Power on the computer and press **** immediately will allow you to enter Setup. The other way to enter Setup is to power on the computer, when the below message appears briefly at the bottom of the screen during the POST (Power On Self Test), press **** key

**TO ENTER SETUP BEFORE BOOT
PRESS KEY**

✓ **Getting Help**

Main Menu

The on-line description of the highlighted setup function is displayed at the bottom of the screen.

Sub-Menu

If you find a right pointer symbol appears to the left of certain fields (as shown in the right view), that means a sub-menu containing additional options for the field can be launched from this field.

▶ IDE Primary Master
▶ IDE Primary Slave
▶ IDE Secondary Master
▶ IDE Secondary Slave

To enter the sub-menu, highlight the field and press **<Enter>**. Then you can use control keys to move between and change the settings of the sub-menu.

To return to the main menu, press **<Esc>** to trace back.

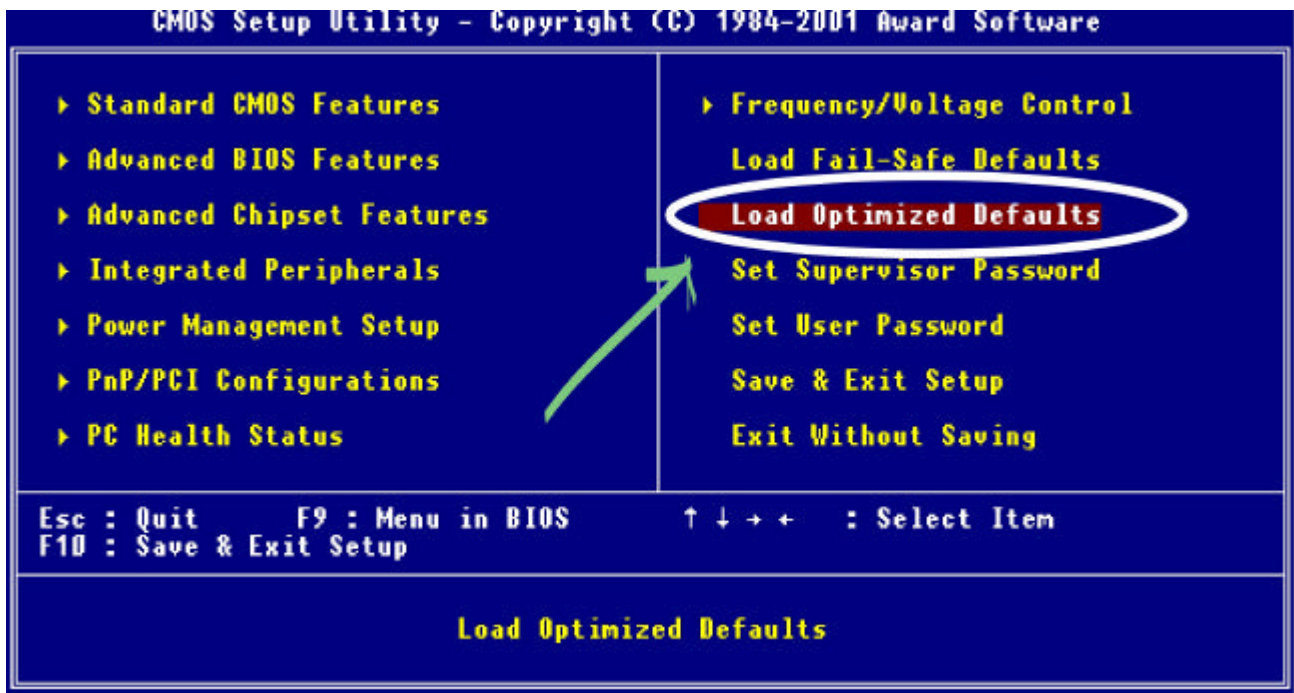
Status Page Setup Menu/Option Page Setup Menu

Press **<F1>** to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press **<Esc>**.

✓ The Main Menu

Once you enter Award BIOS CMOS Setup Utility, the Main Menu (Figure 1) will appear on the screen. The Main Menu allows you to select from ten setup functions and two exit choices. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.

It is recommended to load the Defaults for "Optimized" or "Fail-Safe".



Standard CMOS Features

Use this menu for basic system configuration.

Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

Power Management setup

Use this menu to specify your settings for power management

PNP/PCI Configuration

This entry appears if your system supports PnP / PCI.

PC health Status

Display CPU/System Temperature, Fan speed.

Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

Set Supervisor Password

Enter and change the options of the setup menus. If password error or disable, some read only INFO will be displayed on the menu.

Set User Password

Change, set, or disable password of user while posting. Switched by Security Option Item in Advanced BIOS Features Function.

Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

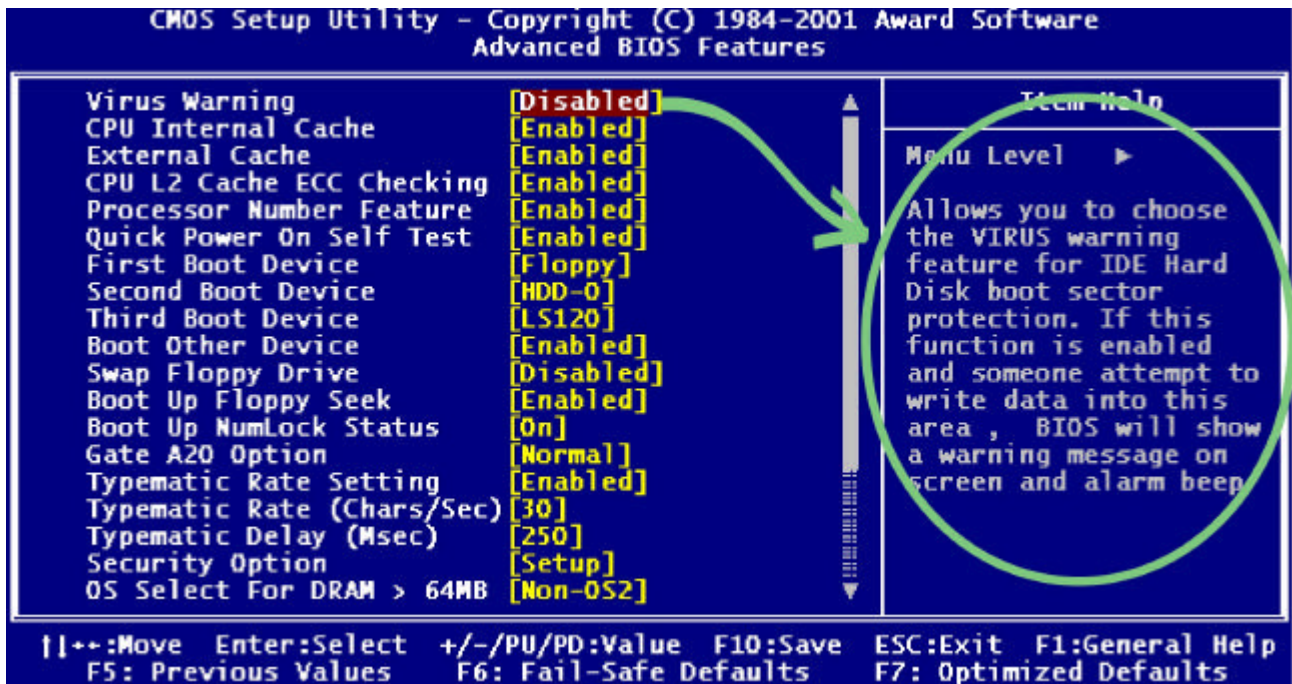
Exit Without Saving

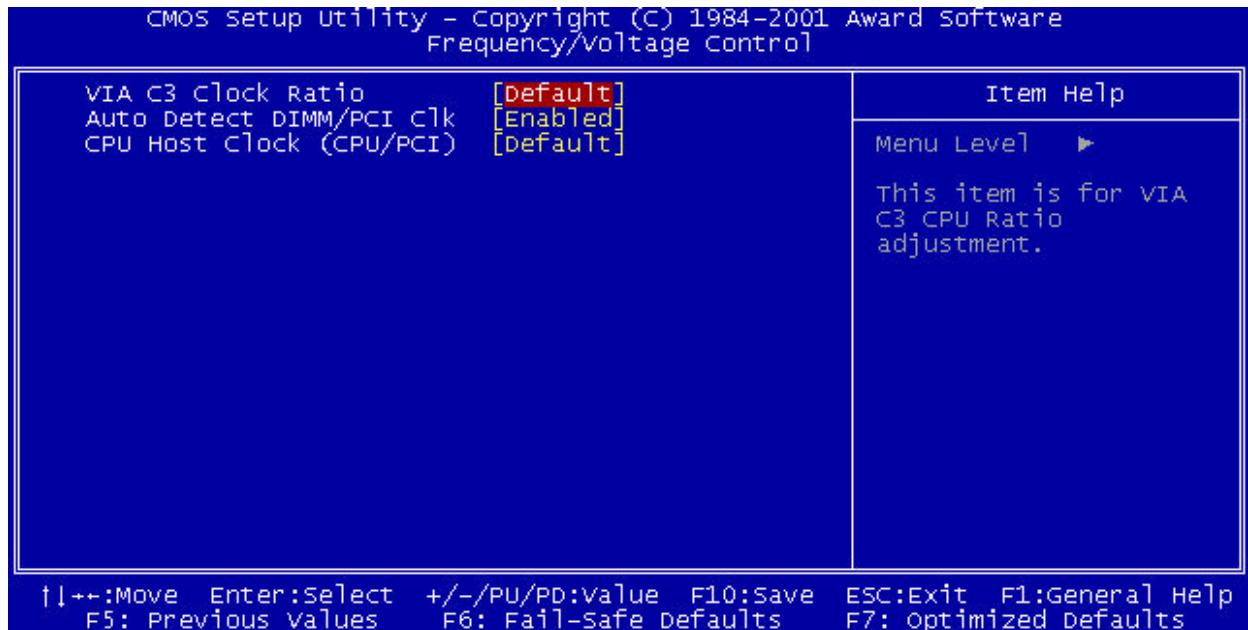
Abandon all CMOS value changes and exit setup.

✓ BIOS Setup Function Description

The New BIOS setup give users a more friendly information, which include all function descriptions of BIOS setup program into the BIOS Flash ROM. When you select one function of BIOS setup program, the function description will appeared at the right side of screen. Hence, user doesn't need read this manual while changing the BIOS setting.

For some critical setting or normal setting, which have no description on the Item Help windows, user can check our Customer Service Department for detail information.





It is highly recommended to use the Default Setting for the CPU Clock Ratio and Host Clock. If the wrong setting for the on board CPU cause the system can't boot up, please Clear CMOS by hardware Jumper to restore factory default value.

✓ **Supervisor/User Password Setting**

You can set either supervisor or user password, or both of them. The differences between are:

Supervisor password

Can enter and change the options of the setup menus.

User password

Just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

✓ **ENTER PASSWORD:**

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

✓ PASSWORD DISABLED

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup.

✓ Power-On Boot

After you have made all the changes to CMOS values and the system cannot boot with the CMOS values selected in Setup, restart the system by turning it OFF then ON or Pressing the "RESET" button on the system case. You may also restart by simultaneously press **<Ctrl>**, **<Alt>**, and **<Delete>** keys.

Upon restart the system, immediately press **<Insert>** to load BIOS default CMOS value for boot up.

Chapter 3 Watch Dog Timer & GPIO Programming Guide

Watch Dog Timer Working Procedure

The Watch Dog Timer (WDT) is a special hardware device monitoring the computer system whether it works normally or not. If not, it will fix up the system.

It contains a receivable 1Hz frequency from South Bridge, can set time, and clear the counter function. When the time is up, the WDT can send Reset or NMI signal. Operator has to write a value into the WDT Configuration Register (Write the control value to the Configuration Port), and clear the WDT counter (read the Configuration Port).

Watch Dog Timer Character and Function

WDT Configuration Port	443	Default at 443
Watch Dog Timer	Disabled Enabled	1. Default at disabled. 2. Enabled for user's programming
WDT time out active for	Reset NMI	Default no setting
WDT Active Time	1 sec/min 2 sec/min 4 sec/min 8 sec/min 16 sec/min 32 sec/min 64 sec/min 128 sec/min	

- **Clear the WDT**

Repeatedly read the WDT Configuration Port and the interval cannot be longer than the present time; otherwise, the WDT will generate NMI or Reset signal for the system.

Note:

Before running the WDT, you must clear the WDT, thus making sure the initial value is Zero before enabling the WDT.

- **WDT Control Register (Write to the WDT Configuration Port)**

You can set the WDT Control Register to control the WDT working mode. The initial value of the WDT Control Register is as follows:

You must plan the following options:

1. Enable or Disable Reset: decide D6 value in 443.
2. Enable or Disable NMI: decide D5 value in 443.
3. Select the time-out intervals of the WDT (decide the values of D2, D1, D0 in 443).
4. Enable or Disable the WDT (decide D7 value in 443).

After finishing the above setting, you must output the Control Register's value to the WDT Configuration Port. Then the WDT will start according to the above setting.

- You should build a mechanism in the program to continue to read the WDT Configuration Port for clearing the WDT before time out.

GPIO Programming Guide

J5: General Purpose I/O Port

Pin No.	Definition
1	Power Output. Note.
2	GND
3	GPI/O A
4	GPI/O B
5	GPI/O C
6	GPI/O D

Note: When JP1 Pin 1 and Pin 2 are short, then J5 Pin 1 output is 5V. When JP1 Pin 2 and Pin 3 are short, then J5 Pin 1 output is 12V.

General purpose Input/output pins on J5 connector are optional I/O pins from the VIA82C686A chipset. The GPOx is for signal output while the GPIx, input. Those pins can be controlled by your software. If you have some devices which need to be controlled by motherboard, you can control your device through GPIO.

The following are the information of the EBC 363 GPIO port address:

- (a1.) GPIA VIA82C686A (GP18), Read Port 0x4049h bit 0,
- (a2.) GPOA VIA82C686A (GPO8), Write Port 0x404Dh bit 0,
- (b1.) GPIB VIA82C686A (GP19), Read Port 0x4049h bit 1,
- (b2.) GPOB VIA82C686A (GP09), Write Port 0x404Dh bit 1,
- (c1.) GPIC VIA82C686A (GPI10), Read Port 0x4049h bit 2,
- (c2.) GPOC VIA82C686A (GPO10), Write Port 0x404Dh bit 2,
- (d1.) GPID VIA82C686A (GPI 11), Read Port 0x4049h bit 3,
- (d2.) GPOD VIA82C686A (GPO11), Write Port 0x404Dh bit 3,

Since input and output pins use the same pins, you have to define the In or Out direction first; then control offset 74 of PCI to ISA Bridge.

bit 5: For GPIOD direction -- >0: Input, 1: Output

bit 4: For GPIOC direction -- >0: Input, 1: Output

bit 3: For GPIOB direction -- >0: Input, 1: Output

bit2: For GPIOA direction -- >0: Input, 1: Output