

**ETX-C400(E)**  
**Intel Celeron Processor**  
**ETX CPU Module**  
**With**  
**AUDIO & VGA & LAN**  
**User's Manual**  
**Version 1.01**

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# Chapter 1. Introduction

ETX-C400(E) is an ETX form factor CPU module based on equipped with a low power consumption and high performance INTEL ULV Celeron 400 processor. It is designed for the system manufacturers, integrators, or VARs to provide reliable and quality performance at a reasonable price.

With its small size and four IO connectors, the ETX CPU module can be easily and securely mounted on to a customized baseboard or ICP's ETX development board. It supports the full functions of an AT & ATX-compatible industrial computer on a single board. It is equipped with a low-power consumption and high-performance INTEL ULV C400 processor.

The VIA® TwisterT PN133T (VT8606) is an INTEL processor system logic north bridge with the addition of 100 MHz capability for both the CPU and SDRAM interfaces. VIA® TwisterT PN133T may be used to implement both desktop and laptop personal computer systems from 100MHz to 133MHz based on C3 (EBGA packing). The primary features of the VIA® TwisterT PN133T-North Bridge are: INTEL ULV C400 CPU (Front Side Bus) Interface (100 MHz), SDRAM Memory Interface (100 / 133MHz), 32-bit PCI with Integrated 2D / 3D graphics accelerator.

The VT686B PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high performance, power-efficient, highly integrated and compatible device that supports both Intel and non-Intel based processors to PCI bus bridge functionality, ensuring a complete Microsoft PC99-compliant PCI/ISA system.

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## 1.1 Specifications

- **CPU:** INTEL ULV Celeron 400 EPGA packing
- **DMA Channels:** 7
- **Interrupt Levels:** 15
- **Chipset:** VIA® VT8606 (Integrated 2D / 3D graphics accelerator, include LVDS 36bit LCD and TV out function [optional, available upon request]) and VT686B
- **System Memory:** One SO-DIMM socket supports up to 512MB SDRAM
- **Ultra ATA/33/66/100 IDE Interface:** Two PCI Enhance IDE hard drives. The south bridge VT686B supports Ultra ATA/33/66/100 IDE interface.
- **Serial Ports:** NS16C550 compatible UART
- **Bi-directional Parallel Port:** IEEE1284 compatible
- **IrDA Port:** Supports fast Infrared function (FIR)
- **USB Port:** Equipped with four USB 1.1 ports
- **Audio:** Onboard AC'97Codec, supports two channel Left/Right Line IN/OUT, MIC IN
- **LAN (ETX-C400E):** Realtek RTL8100BL, IEEE802.3u 100 BASE-TX standard Dual Auto-sensing interface to 10MBps or 100MBps networks.
- **Keyboard Connector & PS/2 Mouse Port on-board**
- **Power Consumption:** +5V @ 1.8A, (Intel Celeron 400MHz with 512MB SO-DIMM, Windows2000) (Option -- Celeron 650MHz CPU, +5V @ 2.4A)
- **Operating Temperature:** 0° - 50° C (CPU needs Cooler)

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## 1.2 Package Contents

In addition to this *User Manual*, the ETX-C400(E) package includes the following items:

- ETX-C400(E) CPU Module x 1
- CD for utilities and drivers x 1
- Installation Guide CD (user manual included) x 1
- Quick Startup Reference x 1

If any of these items are missing or damaged, please contact the dealer from whom you purchased the product. Be sure to save the shipping materials and carton in case you want to ship or store the product in the future.

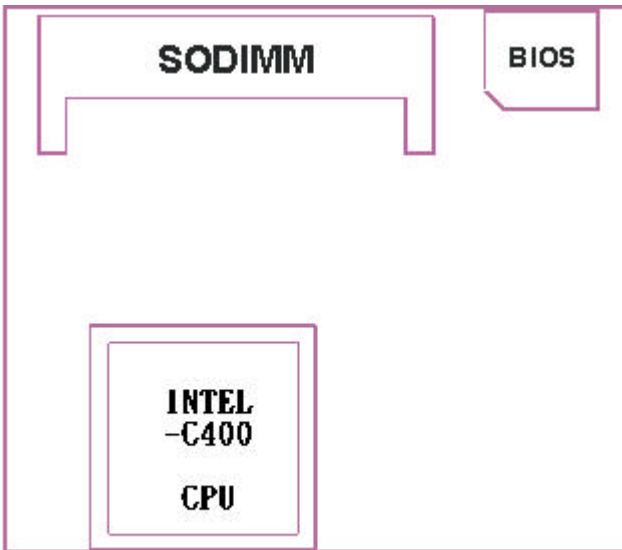
# Chapter 2. Installation

This chapter describes how to install the ETX-C400(E). First a layout diagram of the ETX-C400(E) is shown, followed by unpacking information that should be carefully followed. The jumpers and switch settings for the ETX-C400(E) configuration, such as CPU type selection, system clock setting, and watchdog timer, are also listed.

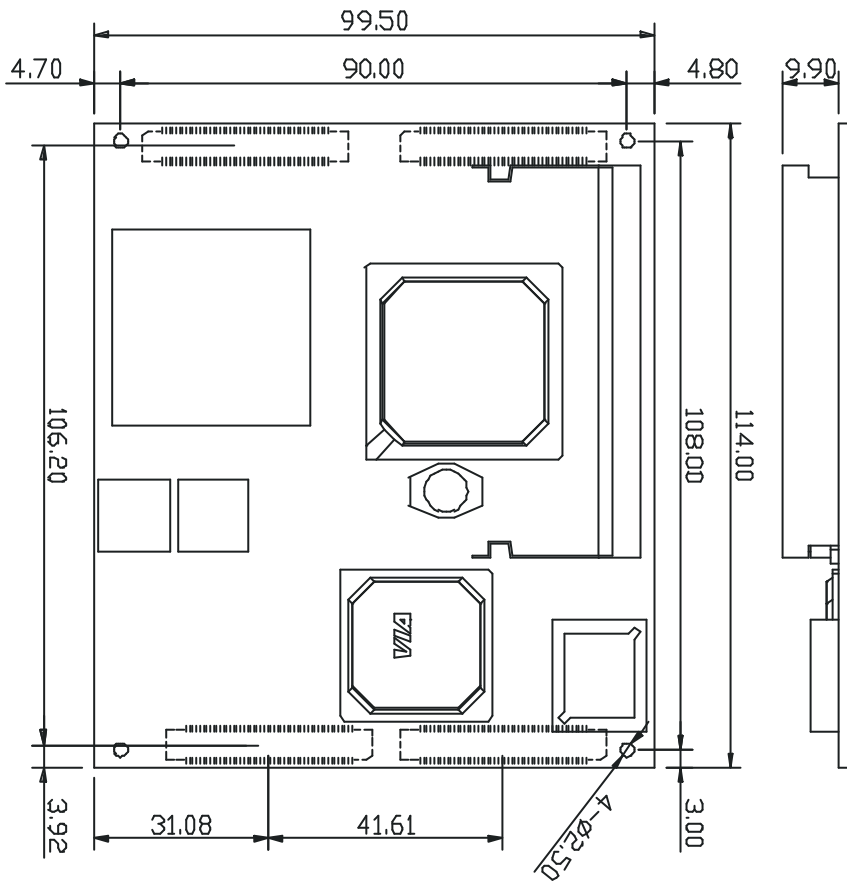
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## 2.1 Layout Diagram & Dimension

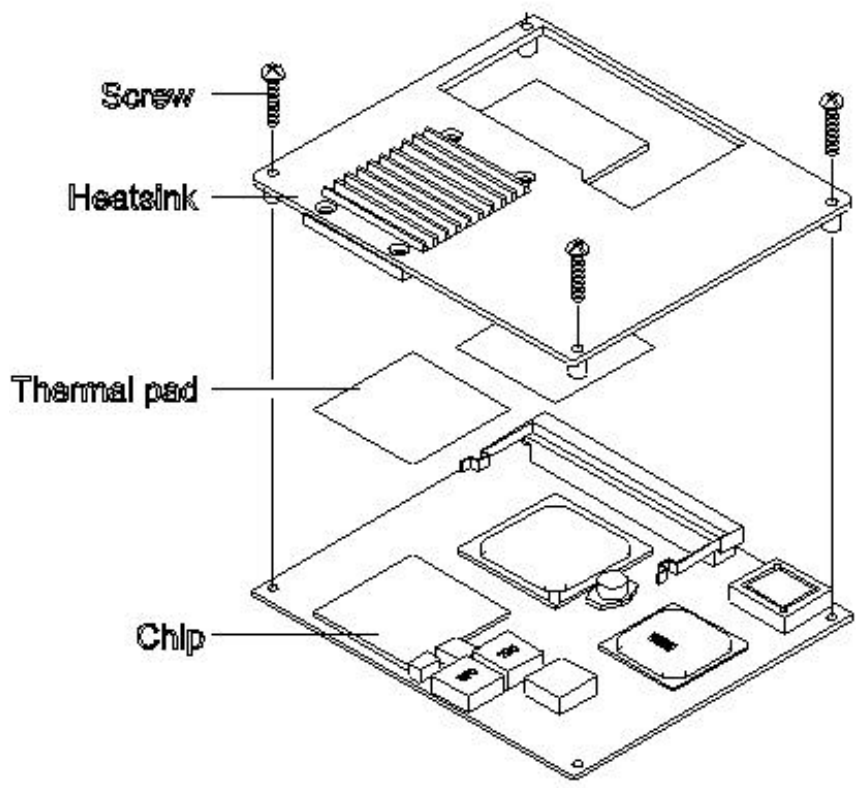
- **Diagram**



- **Dimension**



- **Assemblage**



# Chapter 3. Connection

This chapter describes how to connect peripherals, switches and indicators to the ETX-C400(E) board.

## 3.1 ETX Board X1-X4 Connector

ETX-C400(E) CPU module has four connectors (X1-X4), which are connected to baseboard.

- **X1 Connector: PCI Bus, USB and AUDIO**

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V
13	REQ2#	14	GNT1#
15	REQ1#	16	3V
17	GNT0#	18	RESERVED
19	VCC	20	VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SNDL
47	AD15	48	ASGND

PIN	SIGNAL	PIN	SIGNAL
51	VCC	52	VCC
53	PAR	54	SERR#
55	GPERR#	56	RESERVED
57	PME#	58	USB2
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3
63	IRDY#	64	STOP#
65	FRAME#	66	USB2#
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3#
73	AD19	74	AD18
75	AD20	76	USB0
77	AD22	78	AD21
79	AD23	80	USB1
81	AD24	82	CBE3#
83	VCC	84	VCC
85	AD25	86	AD26
87	AD28	88	USB0#
89	AD27	90	AD29
91	AD30	92	USB1#
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#

49	CBE1#	50	SNDR
----	-------	----	------

99	GND	100	GND
----	-----	-----	-----

• X2 Connector: ISA Bus

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	N.C.
7	SD12	8	DRQ7
9	SD11	10	DACK7#
11	SD10	12	DRQ6
13	SD9	14	DACK6#
15	SD8	16	DRQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DRQ0
21	SA17	22	DACK0#
23	SA18	24	IRQ14
25	SA19	26	IIR15
27	SA20	28	IRQ12
29	SA21	30	IRQ11
31	SA22	32	IRQ10
33	SA23	34	IOCS16#
35	GND	36	GND
37	SBHE#	38	MEMCS16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA1	44	TC
45	SA3	46	DACK2#
47	SA4	48	IRQ3
49	SA5	50	IRQ4

PIN	SIGNAL	PIN	SIGNAL
51	5V	52	5V
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	N.C.
63	SA11	64	REQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DRQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	5V	84	5V
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	ZOWS#
91	DRQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	N.C.	98	RSTDRV
99	GND	100	GND

• X3 Connector: VGA, LCD, Video, COM1, COM2,  
LPT/Floppy, Irda, Mouse and Keyboard

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT #	10	DDDA
11	LCDDO1 6	12	LCDDO1 8
13	LCDDO1 7	14	LCDDO1 9
15	GND	16	GND
17	LCDDO1 3	18	LCDDO1 5
19	LCDDO1 2	20	LCDDO1 4
21	GND	22	GND
23	LCDDO8	24	LCDDO1 1
25	LCDDO9	26	LCDDO1 0
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC	40	VCC
41	JILI_DAT	42	LTGIO0
43	JILI_CLK	44	BLON#
45	BIASON	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

PIN	SIGNAL	PIN	SIGNAL
51	LPT/FLPY#	52	RESERVED
53	VCC	54	GND
55	STB# / RESERVED	56	AFD# / DENSEL
57	RESERVED	58	PD7 / RESERVED
59	IRRX	60	ERR# / HDSEL#
61	IRTX	62	PD6 / RESERVED
63	RXD2	64	INIT# / DR#
65	GND	66	GND
67	RTS2#	68	PD5 / RESERVED
69	DTR2#	70	SLIN# / STEP#
71	DCD2#	72	PD4 / DSKCHG#
73	DSR2#	74	PD3 / RDATA#
75	CTD2#	76	PD2 / WP#
77	TXD2	78	PD1 / TRK0#
79	RI2#	80	PDO / INDEX#
81	VCC	82	VCC
83	RXD1	84	ACK# / DRV
85	RTS1#	86	BUSY# / MOT
87	DTR1#	88	PE / WDATA#
89	DCD1#	90	SLCT# / WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

**\* LVDS PIN DESCRIBE & DEFINITION :**

<i>PIN NAME</i>	<i>LVDS SIGNAL</i>	<i>CHANNEL</i>
LCDDO0	Txout0#	first
LCDDO1	Txout0	first
LCDDO2	Txout1#	first
LCDDO3	Txout1	first
LCDDO4	Txout2#	first
LCDDO5	Txout2	first
LCDDO6	Txclk#	first
LCDDO7	Txclk	first
LCDDO8	N/A	first
LCDDO9	N/A	first
LCDDO10	Txout0#	sceond
LCDDO11	Txout0	sceond
LCDDO12	Txout1#	sceond
LCDDO13	Txout1	sceond
LCDDO14	Txout2#	sceond
LCDDO15	Txout2	sceond
LCDDO16	Txclk#	sceond
LCDDO17	Txclk	sceond
LCDDO18	N/A	sceond
LCDDO19	N/A	sceond

• X4 Connector: IDE1, IDE2, LAN and Miscellaneous

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	RESERVED	10	RESERVED
11	WDTRIG	12	RESERVED
13	RESERVED	14	RESERVED
15	RESERVED	16	RESERVED
17	VCC	18	VCC
19	OVCR#	20	GPCS#
21	EXTSMI#	22	RESERVED
23	SMBCLK	24	SMBDATA
25	SIDE_CS3#	26	RESERVED
27	SIDE_CS1#	28	DASP_S
29	SIDE_A2	30	PIDE_CS3
31	SIDE_A0	32	PIDE_CS1#
33	GND	34	GND
35	PDIAG_S	36	PIDE_A2
37	SIDE_A1	38	PIDE_A0
39	SIDE_INTR Q	40	PIDE_A1
41	RESERVED	42	RESERVED
43	SIDE_AK#	44	PIDE_INTRO
45	SIDE_RDY	46	PIDE_AK#
47	SIDE_IOR#	48	PIDE_RDY
49	VCC	50	VCC

PIN	SIGNAL	PIN	SIGNAL
51	SIDE_IOW#	52	PIDE_IOR#
53	SIDE_DRQ	54	PIDE_IOW #
55	SIDE_D15	56	PIDE_DRQ
57	SIDE_D0	58	PIDE_D15
59	SIDE_D14	60	PIDE_D0
61	SIDE_D1	62	PIDE_D14
63	SIDE_D13	64	PIDE_D1
65	GND	66	GND
67	SIDE_D2	68	PIDE_D13
69	SIDE_D12	70	PIDE_D2
71	SIDE_D3	72	PIDE_D12
73	SIDE_D11	74	PIDE_D3
75	SIDE_D4	76	PIDE_11
77	SIDE_D10	78	PIDE_D4
79	SIDE_D5	80	PIDE_D10
81	VCC	82	VCC
83	SIDE_D9	84	PIDE_D5
85	SIDE_D6	86	PIDE_D9
87	SIDE_D8	88	PIDE_D6
89	RESERVED	90	RESERVED
91	RXD#	92	PIDE_D8
93	RXD	94	SIDE_D7
95	TXD#	96	PIDE_D7
97	TXD	98	HDRST#
99	GND	100	GND

# Chapter 4. BIOS Setup

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## 4.1 Introduction

This chapter discusses the Setup program built into the BIOS, which allows users to configure the system. This configuration is then stored in battery-backed CMOS RAM so that Setup information is retained whilst the power is off.

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## 4.2 Starting Setup

The BIOS will be activated immediately when you turn on the computer. To enter the Setup program when the BIOS system is activated:

1. Press <Del> immediately after switching the system on, or
2. Press <Del> when the following message appears briefly at the bottom of the screen during the POST (Power On Self-Test).

Press DEL to run SETUP.

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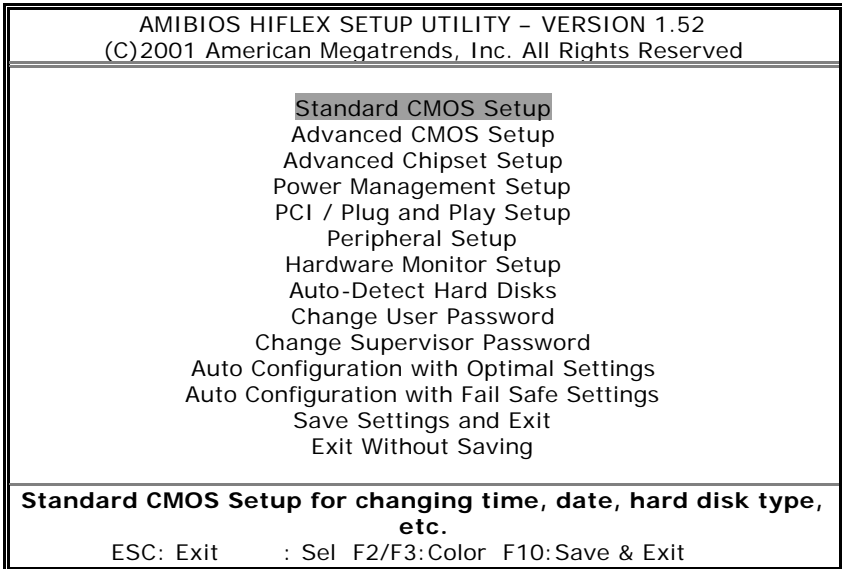
## 4.3 Setup Summary

- **Standard CMOS Setup:**  
Standard CMOS Setup to change time, date, hard disk type, etc.
- **Advanced CMOS Setup:**  
Advanced CMOS Setup to configure system options.
- **Advanced Chipset Setup:**  
Advanced Chipset Setup to configure chipset features.
- **Power Management Setup:**  
Power Management Setup to configure power management features.
- **PCI / Plug and Play Setup:**  
Configures PCI / Plug and Play features.
- **Peripheral Setup:**  
Configures peripheral features.
- **Hardware Monitor Setup:**  
Configures hardware monitor features.
- **Auto-Detect Hard Disks:**  
These options allow the user to configure the drive named in the option. Select Auto-Detect Hard Disks to allow AMIBIOS to automatically configure the drive. A list of drive parameters will appear on the screen.
- **Change User Password:**  
Change the user password.
- **Change Supervisor Password:**  
Change the supervisor password.
- **Auto Configuration with Optimal Settings:**  
Load configuration settings that ensure the highest performance.

- **Auto Configuration with Fail Safe Settings:**  
Load fails-safe configuration settings.
- **Save Settings and Exit:**  
Write the current settings to CMOS and exit.
- **Exit Without Saving:**  
Exit without saving the current settings.

---

## 4.4 Main Menu Selections



**Figure 1: The Main Menu**

## 4.5 Standard CMOS Setup Selections

AMIBIOS SETUP – STANDARD CMOS SETUP							
(C)2001 American Megatrends, Inc. All Rights Reserved							
Date (mm/dd/yyyy): Tue Mar 19,2002				Base Memory: 639 KB			
Time (hh/mm/ss): 17:18:10				Extd Memory: 247 MB			
Floppy Drive A:		Not Installed					
Floppy Drive B:		Not Installed					
	Type	Size	Cyln	Head	LBA BIK PIO 32Bit	WPcom	Sec Mode Mode Mode
Mode							
Pri Master: Auto						On	
Pri Slave : Auto						On	
Sec Master: Auto						On	
Sec Slave : Auto						On	
Boot Sector Virus Protection				Disabled			
Month: Jan – Dec				ESC:Exit :Sel			
Day: 01 – 31				PgUp/PgDn:Modify			
Year: 1980 – 2099				F1:Help F2/F3:Color			

**Figure 2: Standard CMOS Setup**

- **Floppy Drive A or B**

Move the cursor to these fields and select the floppy type.

Primary/Secondary Master/Slave LBA Mode

LBA (Logical Block Addressing) is a new IDE HDD access method developed to overcome the 528-megabyte capacity bottleneck. If your IDE hard disk capacity is larger than 528MB, AMIBIOS can enable this LBA mode feature. The option is only for Primary Master IDE LBA mode.

- **Primary/Secondary Master/Slave Block Mode**

If your hard disk drive supports IDE block transfer mode, enable this option for a faster IDE hard disk drive transfer rate. The option is only for Primary Master Block mode.

- **Primary/Secondary Master/Slave PIO Mode**

This option enables Primary Master IDE PIO mode on the IDE, which can set proper cycle timings. The cycle timing between the IDE PIO mode value and IDE cycle timing is shown below:

Mode 0 -> Timing (600ns) Mode 1 -> Timing (383ns)

Mode 2 -> Timing (240ns) Mode 3 -> Timing (180ns)

Mode 4 -> Timing (120ns) Mode 5 -> Timing (60ns)

- **Primary/Secondary Master/Slave 32Bit Mode**

This option enables Primary Master IDE 32-bit data transfers on the IDE data port. If disabled, 16-bit data transfer is used by the BIOS. 32-bit data transfers can only be activated if IDE prefetch mode is also enabled.

- **Boot Sector Virus Protection**

When this option is enabled, AMIBIOS issues a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. The settings are Disabled, Enabled.

## 4.6 Advanced CMOS Setup Selections

AMIBIOS SETUP - ADVANCED CMOS SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
Quick Boot	Enabled	Available Options: Disabled > Enabled
1st Boot Device	Disabled	
2nt Boot Device	Disabled	
3rd Boot Device	Disabled	
Try Other Boot Devices	Yes	
S.M.A.R.T. for Hard Disks	Disabled	
BootUP Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
PS/2 Mouse Support	Enabled	
System Keyboard	Present	
Primary Display	VGA/EGA	
Boot To OS/2	No	
Wait For 'F1' If Error	Enabled	
Hit 'DEL' Message Display	Enabled	
CPU MicroCode Updation	Enabled	
L1 Cache	Enabled	
L2 Cache	Enabled	ESC:Exit :Sel
System BIOS Cacheabled	Enabled	PgUp/PgDn:Modify
C000 32K Shadow	Cached	F1:Help F2/F3:Color

**Figure 3: Advanced CMOS Setup**

- **S.M.A.R.T. for Hard Disks**

Self-Monitoring, Analysis and Reporting Technology. This option can help the BIOS to warn the user of a possible device failure and give the user a chance to back up the device before the failure actually happens.

The settings are Auto, Disabled, Enabled.

- **Floppy Drive Seek**

Set this option to Enabled to specify that floppy drive A will perform a Seek operation at system boot. The settings are Enabled or Disabled.

- **Quick Boot**

When Quick Boot is selected, DRAM testing function will be disabled.

- **1st Boot Device**

This option sets the type of device for the first boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, and SCSI.

- **2nd Boot Device**

This option sets the type of device for the second boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, and CDROM.

- **3rd Boot Device**

This option sets the type of device for the third boot drives that the

AMIBIOS attempts to boot from after AMIBIOS POST completes.

The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, and CD ROM.

- **Try Other Boot Devices**

Set this option to Yes to instruct AMIBIOS to attempt to boot from any other drive in the system if it cannot find a boot drive among the drives specified in the 1st Boot Device, 2nd Boot Device, 3rd Boot Device, 4th Boot Device options. The settings are Yes or No.

- **BootUp Num-Lock**

When this option is selected, Num Lock is turned off when the system is powered on so the user can use the arrow keys on both the numeric keypad and the keyboard.

- **PS/2 Mouse Support**

When this option is enabled, BIOS supports a PS/2- type mouse.

- **System Keyboard**

This option does not specify if a keyboard is attached to the computer. Rather, it specifies if error messages are displayed if a keyboard is not attached. This option enables you to configure workstation without keyboard. The settings are Absent or Present.

- **Primary Display**

Select this option to configure the type of monitor attached to the computer. The settings are Monochrome, Color 40x25, Color 80x25,VGA/PGA/EGA, or Not Install.

- **Boot To OS/2**

Set this option to Enabled if running OS/2 operating system and when the system memory on the motherboard is larger than . The settings are Disabled or Enabled.

- **Wait For 'F1' If Error**

If this option is enabled, AMIBIOS will wait for the end user to press <F1> before continuing. If this option is disabled, AMIBIOS continues the boot process without waiting for <F1> to be pressed. The settings are Disabled or Enabled.

- **Hit 'DEL' Message Display**  
Disabling this option prevents "Hit <DEL> if you want to run Setup" from appearing when the system boots. The settings are Disabled or Enabled.
- **System BIOS Cacheable**  
When this option is set to Enabled, the System ROM area from F0000-FFFFF is copied (shadowed) to the RAM for faster execution.

AMIBIOS SETUP – ADVANCED CMOS SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
C800 16K Shadow	Disabled	Available Options: > Disabled Enabled Cached
CC00 16K Shadow	Disabled	
D000 16K Shadow	Disabled	
D400 16K Shadow	Disabled	
D800 16K Shadow	Disabled	
DC00 16K Shadow	Disabled	
		ESC: Exit       : Sel PgUp/PgDn: Modify F1: Help F2/F3: Color

**Figure 4: Advanced CMOS Setup**

- **C000, 32K Shadow**

When this option is set to Enabled, the Video ROM area from C0000-C7FFF is copied (shadowed) to the RAM for faster execution.

Enabled: The contents of the video ROM area from C0000h - C7FFFh are copied (shadowed) from the ROM to the RAM for faster execution.

Disabled: The contents of the video ROM are not copied to the RAM.

Cached: The contents of the video ROM area from C0000h - C7FFFh are copied from the ROM to the RAM and can be written to or read from the cache memory.

- **C800, 16K Shadow**

This option enables shadowing of the contents of the ROM area named in the option title. The settings are Enabled, Disabled, and Cached. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

- **CC00, 16K Shadow**

This option enables shadowing of the contents of the ROM area named in the option title. The settings are Enabled, Disabled, and Cached. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

- **D000, 16K Shadow**

This option enables shadowing of the contents of the ROM area named in the option title. The settings are Enabled, Disabled, and Cached. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

- **D400, 16K Shadow**

This option enables shadowing of the contents of the ROM area named in the option title. The settings are Enabled, Disabled, and Cached. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

- **D800, 16K Shadow**

This option enables shadowing of the contents of the ROM area named in the option title. The settings are Enabled, Disabled, and Cached. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

- **DC00, 16 K Shadow**

This option enables shadowing of the contents of the ROM area named in the option title. The settings are Enabled, Disabled, and Cached. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

## 4.7 Advanced Chipset Setup Selections

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
CPU FSB	Auto	Available Options: > Disabled Enabled
CPU Ratio	Auto	
***** DRAM Timing *****		
Configure SDRAM Timing by SPD	Disabled	
DRAM Frequency	133Mhz	
SDRAM CAS# Latency	3	
Memory Hole	Disabled	
AGP Mode	4x	
AGP Read Synchronization	Enabled	
AGP Fast Write	Disabled	
AGP Aperture Size	64MB	
AGP Master 1 W/S Write	Disabled	
AGP Master 1 W/S Read	Disabled	
USB Controller	All USB Port	
USB Device Legacy Support	Disabled	
Port 64/60 Emulation	Disabled	
		ESC:Exit :Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

Figure 5: Advanced Chipset Setup

## 4.8 Power Management Setup Selections

AMIBIOS SETUP - POWER MANAGEMENT SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
ACPI Aware O/S	No	Available Options: > No Yes
ACPI Standby State	S1/POS	
Re-Call VGA BIOS at S3	Enabled	
Resuming	Enabled	
Power Management/APM	Disabled	
Video Power Down Mode	Disabled	
Hard Disk Power Down Mode	Disabled	
Standby Time Out (Minute)	Disabled	
Suspend Time Out (Minute)	50%-56.25%	
Throttle Slow Clock Ratio	Ignore	
Display Activity	Monitor	
IRQ3	Monitor	
IRQ4	Ignore	
IRQ5	Monitor	
IRQ7	Ignore	
IRQ9	Ignore	
IRQ10	Ignore	
IRQ11	Ignore	ESC: Exit :Sel
IRQ13	Monitor	PgUp/PgDn: Modify
IRQ14	Ignore	F1: Help F2/F3: Color
IRQ15		

**Figure 6: Power Management Setup**

- **Power Management/APM**  
Set this option to Enabled to run APM (Advanced Power Management).
- **Video Power Down Mode**  
Set this option to Enabled to allow the BIOS to power down the Video adapter and Monitor.
- **Hard Disk Power Down Mode**  
Set this option to Enabled to allow the BIOS to shut down the Hard Disk.

- **Standby/Suspend Time Out (Minutes)**

This option specifies the length of time of system inactivity (in minutes) before the system enters Standby/Suspend state.

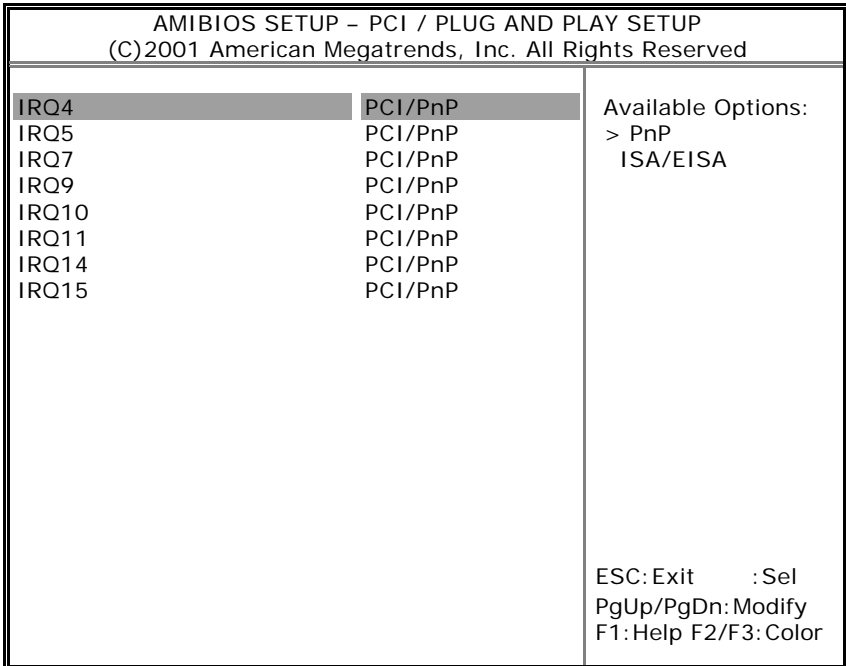
AMIBIOS SETUP - POWER MANAGEMENT SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
Power Button Function	On/Off	Available Options:
Resume On Ring/LAN	Disabled	> On/Off
Resume On LAN	Disabled	Suspend
Resume On RTC Alarm	Disabled	
RTC Alarm Date	15	
RTC Alarm Hour	12	
RTC Alarm Minute	30	
RTC Alarm Second	30	
Power Type Select	AT	
		ESC: Exit      :Sel PgUp/PgDn: Modify F1: Help F2/F3: Color

**Figure 7: Power Management Setup**

## 4.9 PCI / Plug and Play Setup Selections

AMIBIOS SETUP - PCI / PLUG AND PLAY SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	No	Available Options: No > Yes
Clear NVRAM	No	
On Board PCI LAN Controller	Enabled	
OnChip VGA Frame Buffer Size	8MB 32	
PCI Latency Timer (PCI Clocks)	PCI Auto	
Primary Graphics Adapter	0 640x480	
Boot Screen Select	Yes	
LCD Panel Type	Auto	
Allocate IRQ to PCI VGA	Auto	
PCI Slot1 IRQ Priority	Auto	
PCI Slot2 IRQ Priority	Auto	
PCI Slot3 IRQ Priority	PnP	
PCI Slot4 IRQ Priority	PnP	
DMA Channel 0	PnP	
DMA Channel 1	PnP	
DMA Channel 3	PnP	
DMA Channel 5	PnP	
DMA Channel 6	PCI/PnP	
DMA Channel 7		
IRQ3		
		ESC:Exit :Sel PgUp/PgDn: Modif y F1: Help F2/F3: Color

Figure 8: PCI / Plug and Play Setup



**Figure 9: PCI / Plug and Play Setup**

- Plug and Play Aware O/S**  
When this option is enabled, BIOS will configure only PnP ISA boot devices (i.e. all PnP ISA cards which have boot flag set). And PnP aware OS will configure all other devices. When it is disabled, BIOS will configure all devices.
- DMA Channel 0, 1, 3, 5, 6, 7**  
The option enables the user to specify the bus type used by each DMA channel. The settings are PnP or ISA/EISA.
- IRQ3, 4, 5, 7, 9, 10, 11, 14, 15**  
The option specifies the bus on which the specified IRQ line is used. The user can reserve IRQs for legacy ISA adapter cards. At the same time, the user can determine if AMIBIOS should remove an IRQ from all available IRQs

passed to devices configurable by the BIOS system. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs need to be removed, the user can reserve the IRQ by assigning an ISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP.

## 4.10 Peripheral Setup Selections

AMIBIOS SETUP - PERIPHERAL SETUP		
(C)2001 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Enabled	Available Options: Disabled > Enabled
OnBoard Serial Port1	3F8/COM1	
OnBoard FIR Port	Disabled	
FIR IRQ Select	N/A	
FIR DMA1 Select	N/A	
FIR Single DMA Channel	N/A	
FIR DMA2 Select	N/A	
OnBoard Parallel Port	378	
Parallel Port Mode	Normal	
EPP Version	N/A	
Parallel Port DMA	N/A	
Parallel Port IRQ	7	
OnBoard IDE	Both	
OnBoard LAN	Enabled	
OnBoard LAN P.M.E	Enabled	
OnBoard AC' 97 Audio	Enabled	
		ESC: Exit      :Sel PgUp/PgDn: Modify F1: Help F2/F3: Color

**Figure 10: Peripheral Setup**

- **On-Board Parallel Port**  
This option specifies the base I/O port address of the parallel port on the motherboard. The settings are Disabled, 378h, 278h, or 3BCh.

- **Parallel Port Mode**

This option specifies the parallel port mode. The settings are Normal, Bi-Dir, ECP, and EPP.

Normal: The normal parallel port mode is used.

Bi-Dir: Use this setting to support bi-directional transfers on the parallel port.

EPP: The parallel port can be used with devices that adhere to Enhanced Parallel Port (EPP) specifications. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.

ECP: The parallel port can be used with devices adhered to Extended Capabilities Port (ECP) specifications. ECP uses the DMA protocol to achieve data transfer rates of up to 2.5 Megabits per second. ECP also provides symmetric bi-directional communication.

- **Parallel Port IRQ**

This option specifies the IRQ used by the parallel port. The settings are (IRQ)5 and (IRQ)7.

- **Parallel Port DMA Channel**

This option is only available if the setting for the Parallel Port Mode option is set to ECP. It sets the DMA channel used by the parallel port. The available settings are DMA Channel 0, 1, or 3.

---

## 4.11 Hardware Monitor Setup Selections

AMIBIOS SETUP - HARDWARE MONITOR SETUP	
(C)2001 American Megatrends, Inc. All Rights Reserved	
= System Hardware Monitor =	
System Temperature	31°C/87°F
CPU Fan Speed	6300 RPM
+ 2.500V	2.625 V
+ 5.000V	5.070 V
+12.000V	12.046 V
ESC: Exit : Sel	
PgUp/PgDn: Modify	
F1: Help	
F2/F3: Color	

Figure 11: Hardware Monitor Setup

# Appendix A: Address Mapping

## IO Address Map

<b>I/O Address Range</b>	<b>Description</b>
000-01F	DMA Controller #1
020-021	Interrupt Controller #1, Master
040-05F	8254 timer
060-06F	8042 (Keyboard Controller)
070-07F	Real time Clock, NMI Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller #2
0C0-0DF	DMA Controller #2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F2	Core logic programming configuration
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2 (LPT3)
2E8-2EF	Serial Port 4
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1 (LPT2)
3B0-3BF	Monochrome Display and Printer Adapter (LPT1)
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3E8-3EF	Serial Port 3
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

## 1st MB Memory Address Map

Memory address	Description
00000-9FFFF	System memory
A0000-BFFFF	VGA buffer
C0000-C7FFF	VGA BIOS
F0000-FFFFF	System BIOS
1000000-	Extend BIOS

\*Default setting

## IRQ Mapping Table

IRQ0	System Timer	IRQ8	RTC clock
IRQ1	Keyboard	IRQ9	Available
IRQ2	Cascade to IRQ Controller	IRQ10	Available
IRQ3	COM2	IRQ11	Available
IRQ4	COM1	IRQ12	PS2 mouse
IRQ5	Available	IRQ13	FPU
IRQ6	FDC	IRQ14	Primary IDE
IRQ7	Printer	IRQ15	Secondary IDE

## DMA Channel Assignments

Channel	Function
0	Available
1	Available
2	Floppy disk ( 8-bit transfer )
3	Available
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

# Appendix B: Watchdog Timer

The Watchdog Timer is a device to ensure that standalone systems can always recover from abnormal conditions that cause the system to crash. These conditions may result from an external EMI or a software bug. When the system stops working, hardware on the board will perform hardware reset (cold boot) to bring the system back to a known state.

Three I/O ports control the operation of Watchdog Timer.

443 (hex)	Write	Set Watchdog Time period
443 (hex)	Read	Enable the Watchdog Timer.
043/843 (hex)	Read	Disable the Watchdog Timer.

Prior to enable the Watchdog Timer, user has to set the time-out period. The resolution of the timer is 1 second and the range of the timer is 1 sec to 255 sec. You need to send the time-out value to the I/O port – 443H, and then enable it by reading data from the same I/O port – 443H. This will activate the timer that will eventually time out and reset the CPU board. To ensure that this reset condition will not occur, Watchdog Timer must be periodically refreshed by reading the same I/O port 443H. This must be done within the time-out period set by the software. Please refer to the sample program. Finally, we have to disable Watchdog timer by reading the I/O port – 843H or 043H. Otherwise the system could reset unconditionally.

---

*A tolerance of at least 5% must be maintained to avoid unknown routines in the operating system (DOS), such as disk I/O. For example, if the time-out period is set to 10 seconds, the I/O port 443H must be read within 7 seconds.*

---

## Example Assembly Program:

```
TIMER_PORT = 443H
TIMER_START = 443H
TIMER_STOP = 843H
;;INITIAL TIMER COUNTER
MOV DX, TIMER_PORT
MOV AL, 8 ;;8 seconds
OUT DX, AL
MOV DX, TIMER_START
IN AL, DX. ;;START COUNTER
W_LOOP:
MOV DX, TIMER_STOP
IN AL, DX
MOV DX, TIMER_START
IN AL, DX ;;RESTART COUNTER
;;ADD YOUR APPLICATION HERE
CMP EXIT_AP, 0
JNE W_LOOP
MOV DX, TIMER_STOP
IN AL, DX
;;EXIT AP
```